

Enrico/Caruso 15" UMA Schematics Document

Sandy Bridge

Intel PCH

2011-06-02

REV : A00

www.aitech1.ru

DY :None Installed
PSL:10mW internal schematic
10mW: 10mW schematic installed
Surge: Surege schematic installed
GIGA: GIGA schematic installed
10/100: 10/100 schematic installed
HDMI: HDMI schematic installed
Debug: Debug schematic installed

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Enrico/Caruso 15 HR

Rev

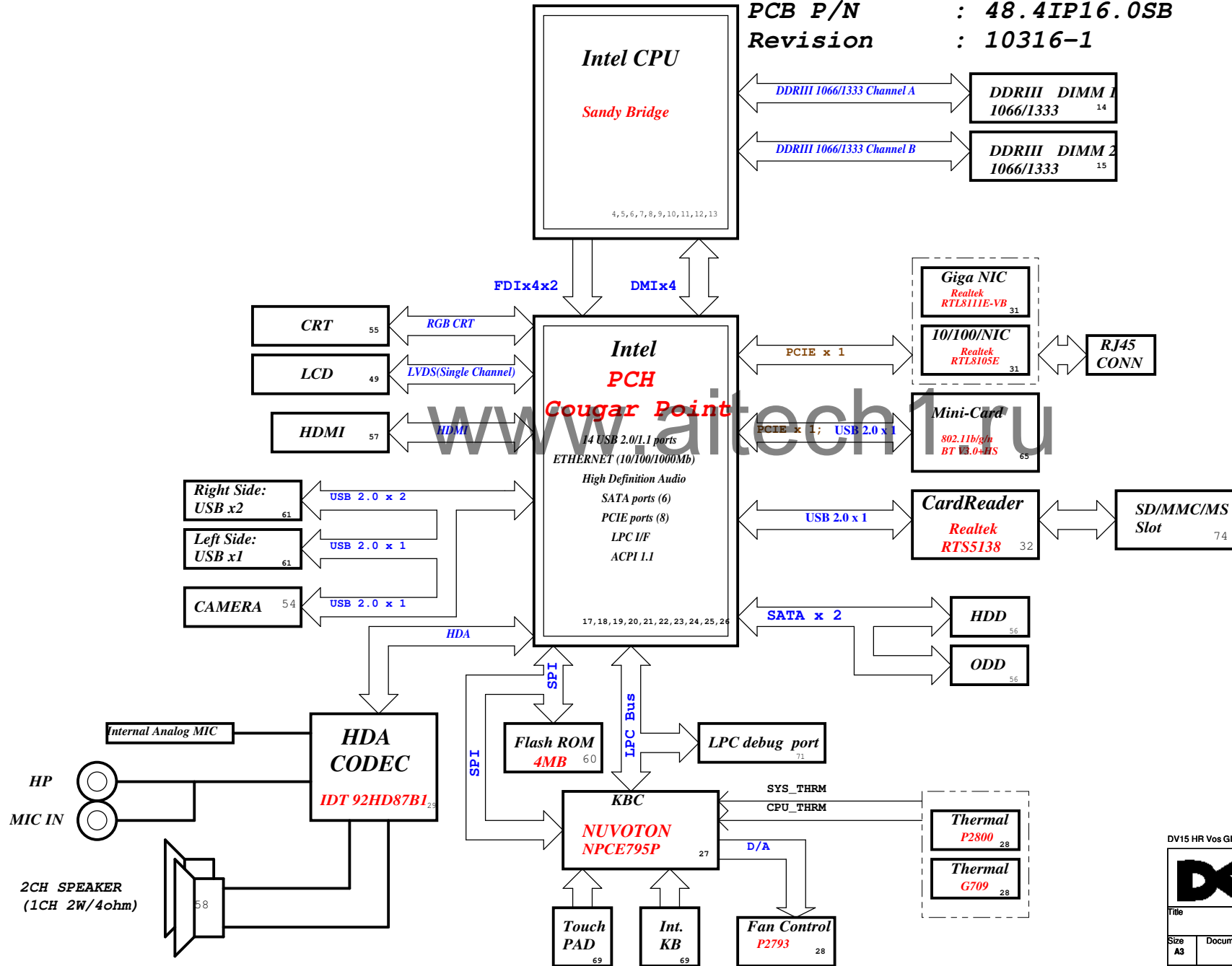
X01

Date: Thursday, June 02, 2011

Sheet 1 of 104

DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001
PCB P/N : 48.4IP16.0SB
Revision : 10316-1



SYSTEM DC/DC	
TPS51461	48
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC	
ISL95831HRTZ	42~44
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

GFX DC/DC	
ISL95831HRTZ	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC	
TPS51218	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC	
TPS51123RGER	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC	
TPS51216RUKR	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

MAXIM CHARGER	
BQ24707	40
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC	
TPS51311RGTR	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER	
L1:Top	L4:Signal
L2:GND	L5:VCC
L3:Signal	L6:Bottom

DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**
Size: A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**
Date: Thursday, June 02, 2011 Sheet: 2 of 104

PCH Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Processor Strapping Huron River Schematic Checklist Rev.0_7


Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 0D8_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB
Device	Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

OV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Table of Content

Size A3

Document Number

Date: Thursday, June 02, 2011

Enrico/Caruso 15 HR

Rev X01

Sheet 3 of 104

5

2



DELL

Title			
CPU (PCIE/DMI/FDI)			
Size A3	Document Number		Rev
	Enrico/Caruso 15 HR		X01
Date:	Thursday, June 02, 2011	Sheet 4 of	104

SSID = CPU

CRB : 47pf
CEKLT: 43pf

www.aitech1.ru

Buffered reset to CPU

Component List:

Ref	Value	Footprint	Notes
R501	62R2J-GP	0603	
C502	SC47P50V2JN-3GP	0603	
R513	56R2J-4-GP	0603	
R504	10KR2J-3-GP	0603	
R505	10KR2J-3-GP	0603	
R510	1K5R2F-2-GP	0603	
R509	750R2F-GP	0603	
R518	10KR2J-3-GP	0603	
C503	SC47P50V2JN-3GP	0603	
R517	10KR2J-3-GP	0603	
R515	10KR2J-3-GP	0603	
RN501	SRN51J-1-GP	0603	
R511	51R2J-2-GP	0603	
R516	10KR2J-3-GP	0603	

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Component List (continued):

Ref	Value	Footprint	Notes
TP501	TP501	0603	
TP502	TP502	0603	
TP503	TP503	0603	
TP504	TP504	0603	
TP505	TP505	0603	
TP506	TP506	0603	
TP507	TP507	0603	
TP508	TP508	0603	
TP509	TP509	0603	
TP510	TP510	0603	
TP511	TP511	0603	
TP512	TP512	0603	

Signal Routing Guideline (continued):
XDP_DBRESET# keep routing length less than 500 mils.

Component List (continued):

Ref	Value	Footprint	Notes
TP503	TP503	0603	
TP504	TP504	0603	
TP505	TP505	0603	
TP506	TP506	0603	
TP507	TP507	0603	
TP508	TP508	0603	
TP509	TP509	0603	
TP510	TP510	0603	
TP511	TP511	0603	
TP512	TP512	0603	

Signal Routing Guideline (continued):
XDP_DBRESET# keep routing length less than 500 mils.

Component List (continued):

Ref	Value	Footprint	Notes
TP503	TP503	0603	
TP504	TP504	0603	
TP505	TP505	0603	
TP506	TP506	0603	
TP507	TP507	0603	
TP508	TP508	0603	
TP509	TP509	0603	
TP510	TP510	0603	
TP511	TP511	0603	
TP512	TP512	0603	

Signal Routing Guideline (continued):
XDP_DBRESET# keep routing length less than 500 mils.

Component List (continued):

Ref	Value	Footprint	Notes
TP503	TP503	0603	
TP504	TP504	0603	
TP505	TP505	0603	
TP506	TP506	0603	
TP507	TP507	0603	
TP508	TP508	0603	
TP509	TP509	0603	
TP510	TP510	0603	
TP511	TP511	0603	
TP512	TP512	0603	

Signal Routing Guideline (continued):
XDP_DBRESET# keep routing length less than 500 mils.

Component List (continued):

Ref	Value	Footprint	Notes
TP503	TP503	0603	
TP504	TP504	0603	
TP505	TP505	0603	
TP506	TP506	0603	
TP507	TP507	0603	
TP508	TP508	0603	
TP509	TP509	0603	
TP510	TP510	0603	
TP511	TP511	0603	
TP512	TP512	0603	

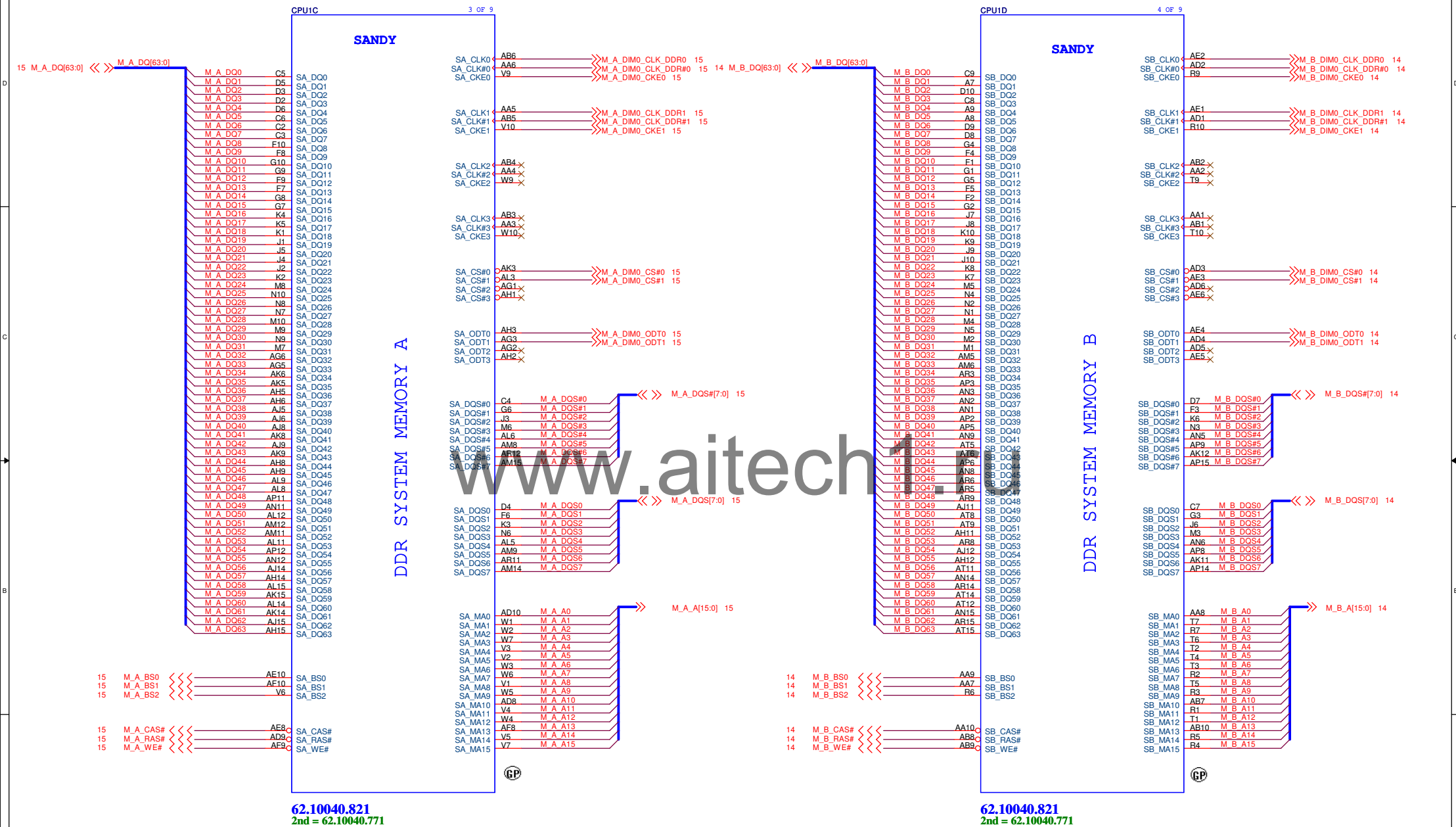
Signal Routing Guideline (continued):
XDP_DBRESET# keep routing length less than 500 mils.

Component List (continued):

Ref	Value	Footprint	Notes
TP503	TP503	0603	
TP504	TP504	0603	
TP505	TP505	0603	
TP506	TP506	0603	
TP507	TP507	0603	
TP508	TP508	0603	
TP509	TP509	0603	
TP510	TP510	0603	
TP511	TP511	0603	
TP512	TP512	0603	

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU (THERMAL/CLOCK/PM)			
Size A3	Document Number	Enrico/Caruso 15 HR	
Date	Thursday, June 02, 2011	Sheet	5 of 104
		X01	

SSID = CPU



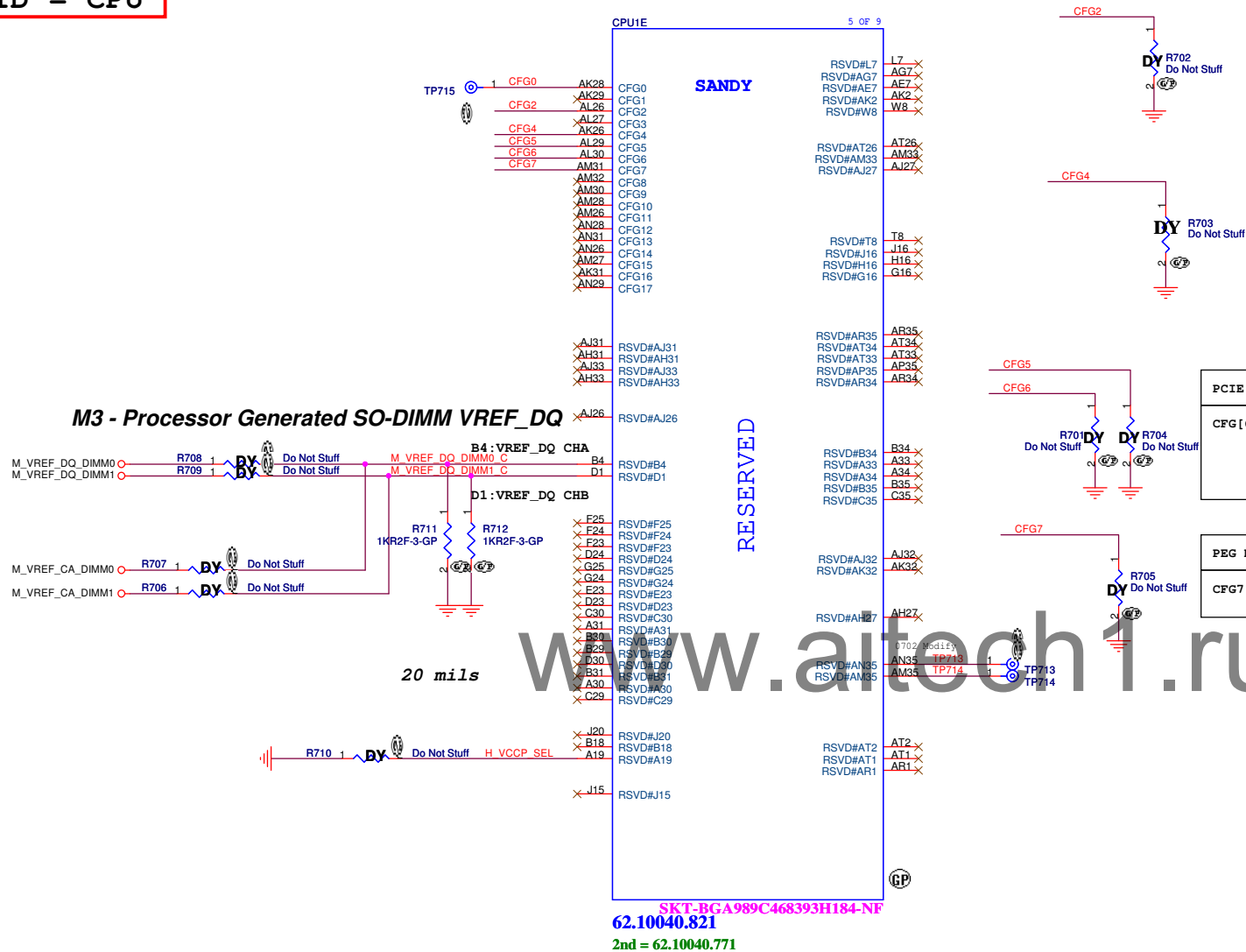
DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (DDR)		
Size	Document Number				Rev
A3	Enrico/Caruso 15 HR				X01
Date:	Thursday, June 02, 2011		Sheet	6	of 104

SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (RESERVED)			
Size A3	Document Number		Rev
	Enrico/Caruso 15 HR		X01
Date:	Thursday, June 02, 2011	Sheet 7 of	104

SSID = CPU

POWER

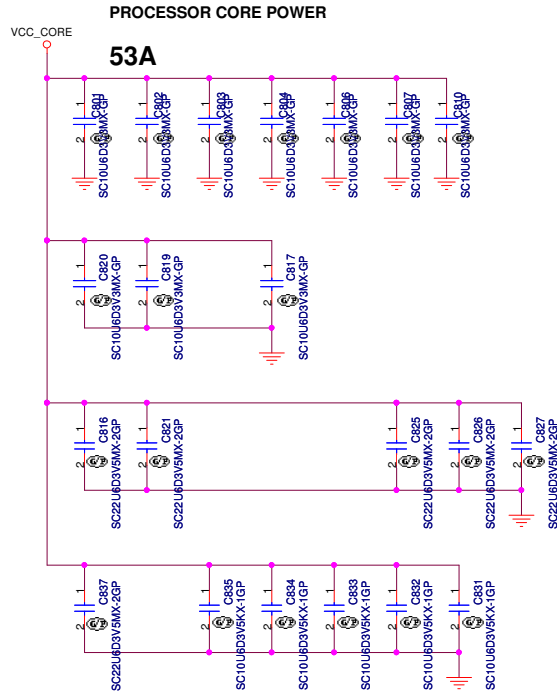
SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

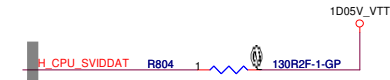
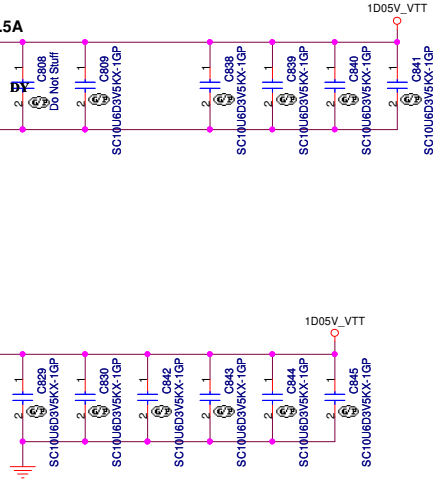


VCC_CORE

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AD26 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
AC29 VCC
AC28 VCC
AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
AA33 VCC
AA32 VCC
AA31 VCC
AA30 VCC
AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
U35 VCC
U34 VCC
U33 VCC
U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

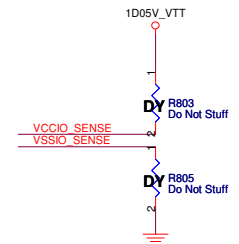
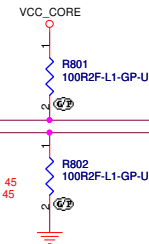
VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO Y10
VCCIO U10
VCCIO P10
VCCIO L10
VCCIO J14
VCCIO J13
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO E11
VCCIO E14
VCCIO E12
VCCIO E11
VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
VCCIO C11
VCCIO B14
VCCIO B12
VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11
VCCIO J23

PROCESSOR VCCIO: 8.5A



VIDALERT# H.CPU_SVIDALRT# R806 1 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK H.CPU_SVIDCLK R806 1 43R2J-GP H.CPU_SVIDCLK 42
VIDSOUT H.CPU_SVIDDAT R806 1 43R2J-GP H.CPU_SVIDDAT 42

VCC_SENSE VSS_SENSE A135 VCCSENSE 42
VCC_SENSE VSS_SENSE A134 VSSSENSE 42
VCCIO_SENSE VSSIO_SENSE B10 VCCIO_SENSE 45
VCCIO_SENSE VSSIO_SENSE A10 VSSIO_SENSE 45



DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

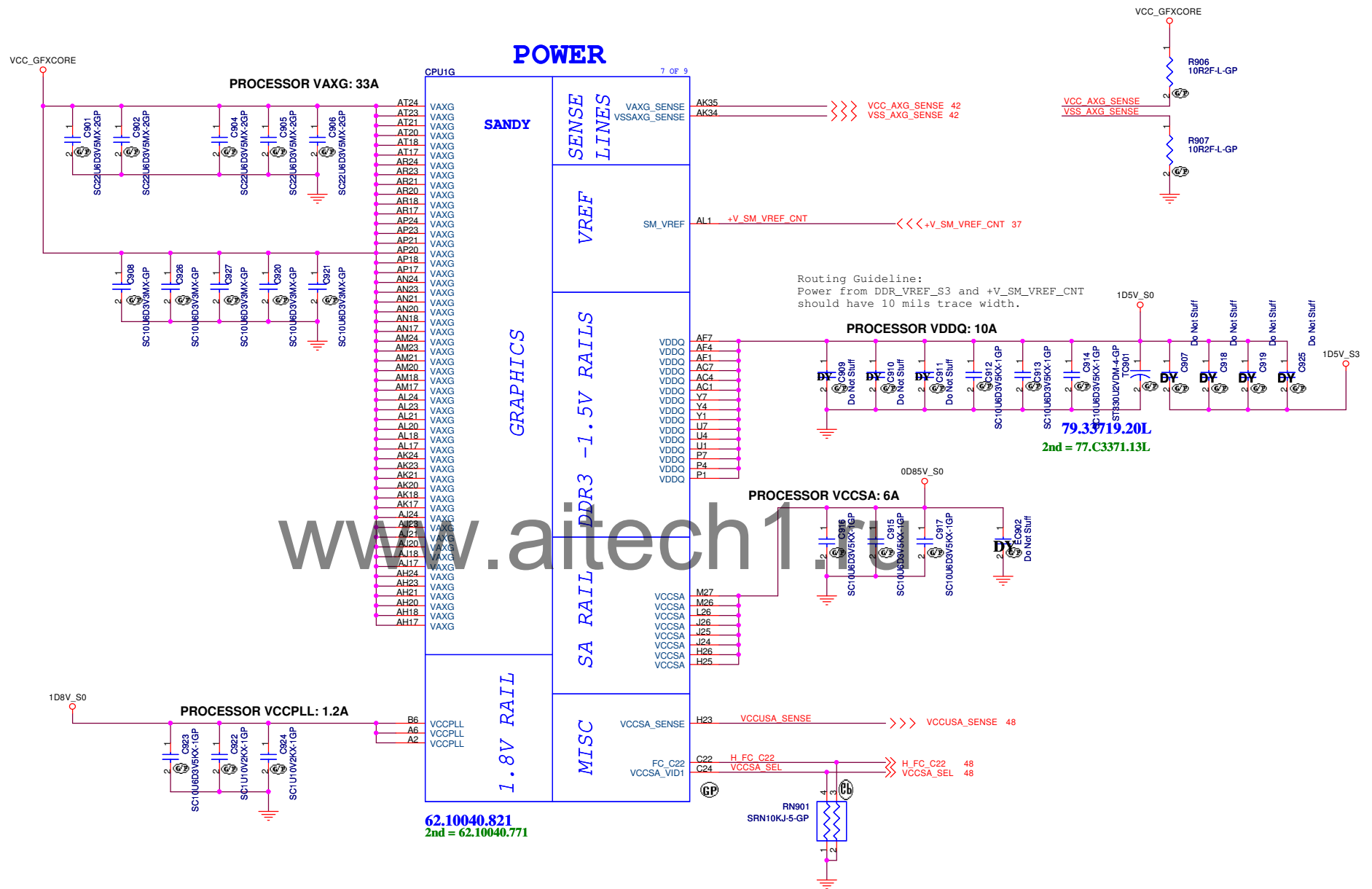
Title **CPU (VCC CORE)**

Size Custom Document Number **Enrico/Caruso 15 HR** Rev **X01**

Date Thursday, June 02, 2011 Sheet 8 of 104

62.10040.821
2nd = 62.10040.771

SSID = CPU



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VCC_GFXCORE)

Size

Document Number	
-----------------	--

Enrico/Caruso 15 HR

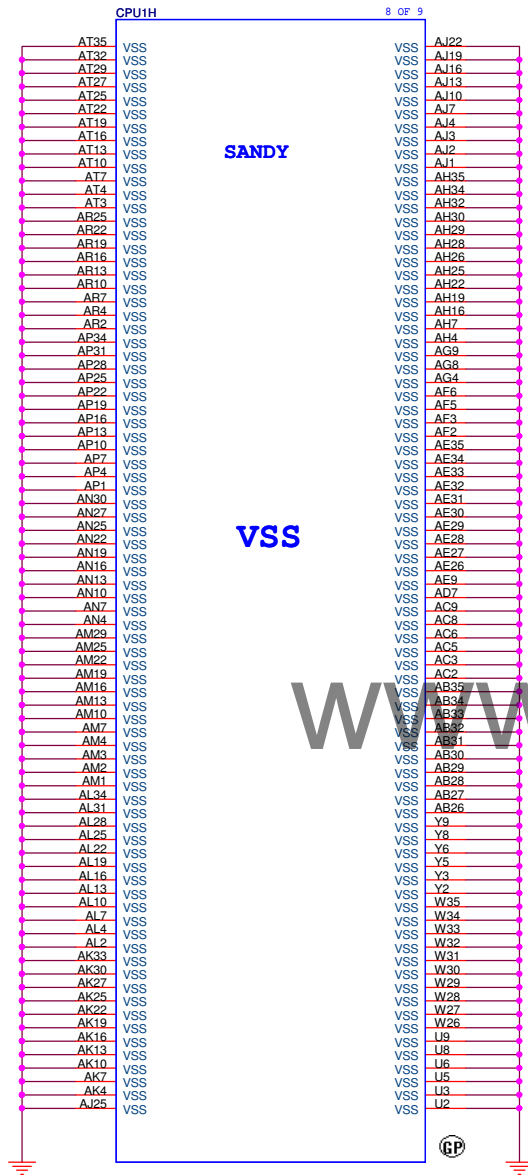
Rev	
-----	--

Date:

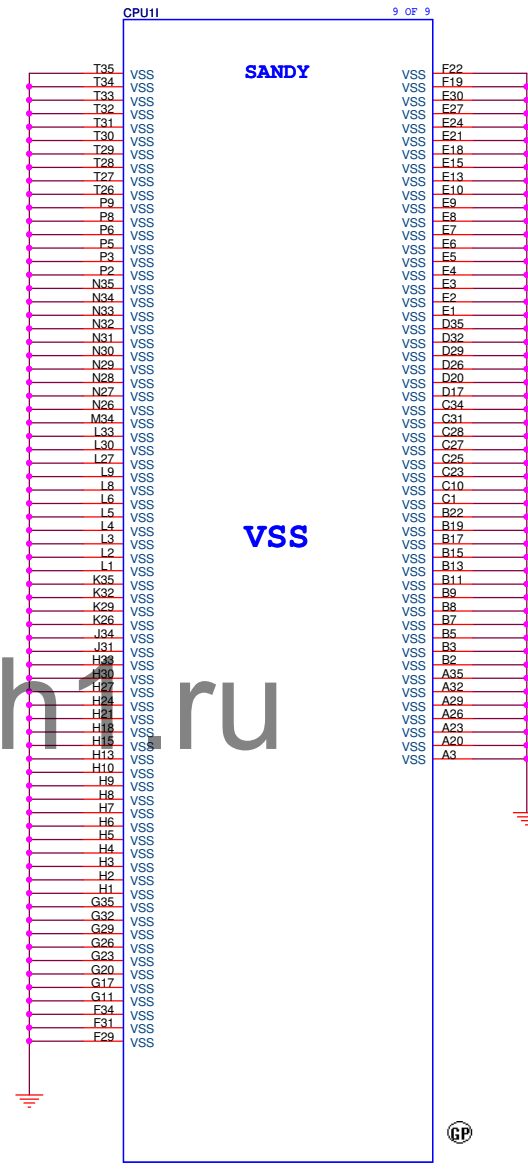
Thursday, June 02, 201

Sheet	9	of	104
-------	---	----	-----

SSID = CPU



62.10040.821
2nd = 62.10040.771



62.10040.821
2nd = 62.10040.771

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (VSS)		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 10	of 104

www.aitech1.ru



XDP

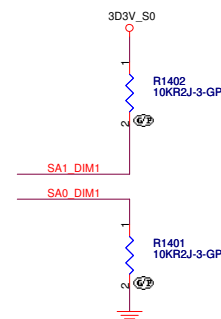
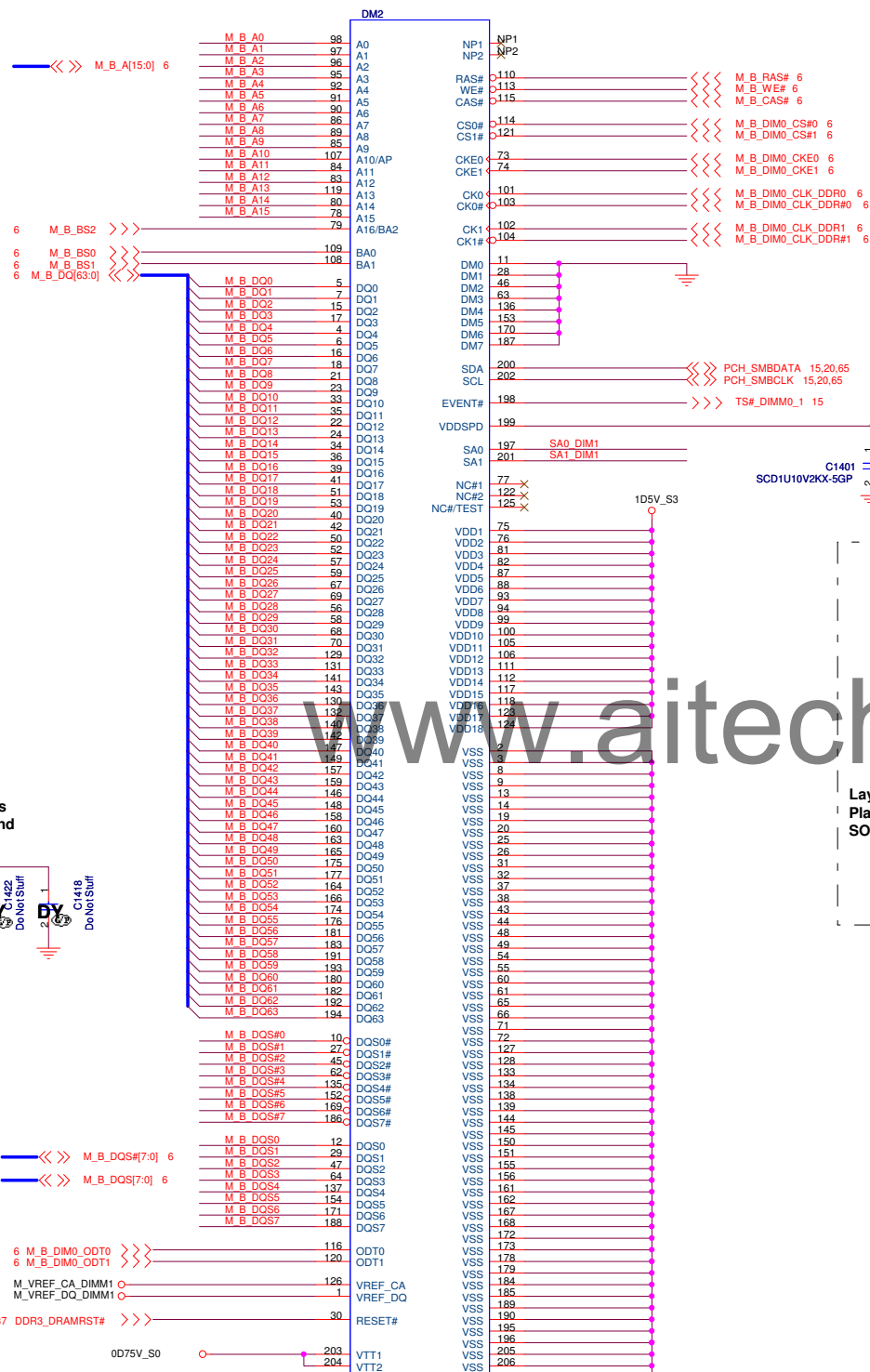
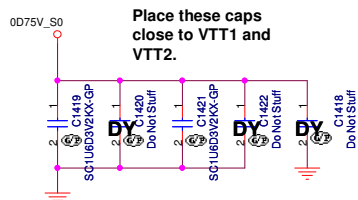
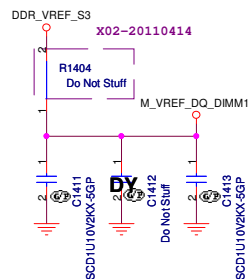
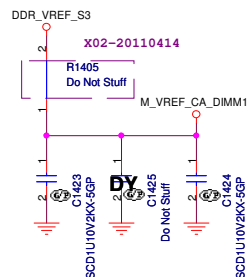
X01

Sheet 11 of 104

www.aitech1.ru

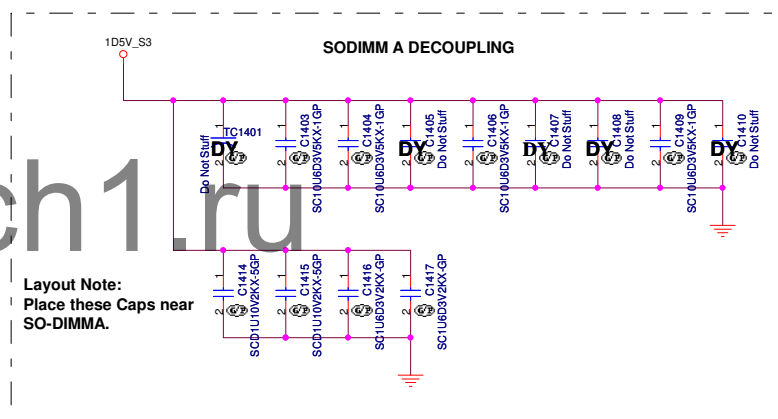
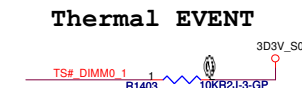
www.aitech1.ru

SSID = MEMORY



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

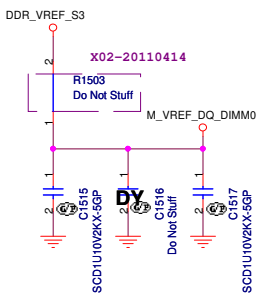
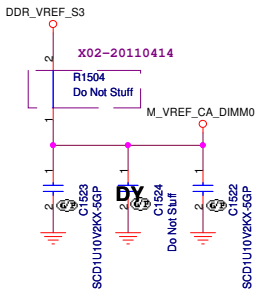


Layout Note:
Place these Caps near
SO-DIMMA.

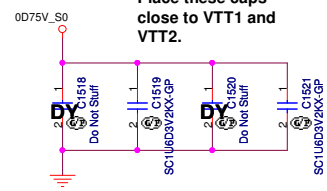
SSID = MEMORY

<< >> M_A_A[15:0] 6

6 M_A_BS2 >>>
6 M_A_BS0 >>>
6 M_A_BS1 >>>
6 M_A_DQ[63:0] >>>



Place these caps close to VTT1 and VTT2.



<< >> M_A_DQS#[7:0] 6
<< >> M_A_DQS#[7:0] 6

6 M_A_DIM0_ODT0 >>>
6 M_A_DIM0_ODT1 >>>

M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

14.37 DDR3_DRAMRST# >>>


0D75V_S0

M_A A0	98	A0
M_A A1	97	A1
M_A A2	96	A2
M_A A3	95	A3
M_A A4	94	A4
M_A A5	93	A5
M_A A6	92	A6
M_A A7	91	A7
M_A A8	90	A8
M_A A9	89	A9
M_A A10	88	A10
M_A A11	87	A11
M_A A12	86	A12
M_A A13	85	A13
M_A A14	84	A14
M_A A15	83	A15
M_A A16	82	A16
M_A A17	81	A17
M_A A18	80	A18
M_A A19	79	A19
M_A A20	78	A20
M_A A21	77	A21
M_A A22	76	A22
M_A A23	75	A23
M_A A24	74	A24
M_A A25	73	A25
M_A A26	72	A26
M_A A27	71	A27
M_A A28	70	A28
M_A A29	69	A29
M_A A30	68	A30
M_A A31	67	A31
M_A A32	66	A32
M_A A33	65	A33
M_A A34	64	A34
M_A A35	63	A35
M_A A36	62	A36
M_A A37	61	A37
M_A A38	60	A38
M_A A39	59	A39
M_A A40	58	A40
M_A A41	57	A41
M_A A42	56	A42
M_A A43	55	A43
M_A A44	54	A44
M_A A45	53	A45
M_A A46	52	A46
M_A A47	51	A47
M_A A48	50	A48
M_A A49	49	A49
M_A A50	48	A50
M_A A51	47	A51
M_A A52	46	A52
M_A A53	45	A53
M_A A54	44	A54
M_A A55	43	A55
M_A A56	42	A56
M_A A57	41	A57
M_A A58	40	A58
M_A A59	39	A59
M_A A60	38	A60
M_A A61	37	A61
M_A A62	36	A62
M_A A63	35	A63
M_A A64	34	A64
M_A A65	33	A65
M_A A66	32	A66
M_A A67	31	A67
M_A A68	30	A68
M_A A69	29	A69
M_A A70	28	A70
M_A A71	27	A71
M_A A72	26	A72
M_A A73	25	A73
M_A A74	24	A74
M_A A75	23	A75
M_A A76	22	A76
M_A A77	21	A77
M_A A78	20	A78
M_A A79	19	A79
M_A A80	18	A80
M_A A81	17	A81
M_A A82	16	A82
M_A A83	15	A83
M_A A84	14	A84
M_A A85	13	A85
M_A A86	12	A86
M_A A87	11	A87
M_A A88	10	A88
M_A A89	9	A89
M_A A90	8	A90
M_A A91	7	A91
M_A A92	6	A92
M_A A93	5	A93
M_A A94	4	A94
M_A A95	3	A95
M_A A96	2	A96
M_A A97	1	A97
M_A A98	0	A98
M_A A99	0	A99
M_A A100	0	A100
M_A A101	0	A101
M_A A102	0	A102
M_A A103	0	A103
M_A A104	0	A104
M_A A105	0	A105
M_A A106	0	A106
M_A A107	0	A107
M_A A108	0	A108
M_A A109	0	A109
M_A A110	0	A110
M_A A111	0	A111
M_A A112	0	A112
M_A A113	0	A113
M_A A114	0	A114
M_A A115	0	A115
M_A A116	0	A116
M_A A117	0	A117
M_A A118	0	A118
M_A A119	0	A119
M_A A120	0	A120
M_A A121	0	A121
M_A A122	0	A122
M_A A123	0	A123
M_A A124	0	A124
M_A A125	0	A125
M_A A126	0	A126
M_A A127	0	A127
M_A A128	0	A128
M_A A129	0	A129
M_A A130	0	A130
M_A A131	0	A131
M_A A132	0	A132
M_A A133	0	A133
M_A A134	0	A134
M_A A135	0	A135
M_A A136	0	A136
M_A A137	0	A137
M_A A138	0	A138
M_A A139	0	A139
M_A A140	0	A140
M_A A141	0	A141
M_A A142	0	A142
M_A A143	0	A143
M_A A144	0	A144
M_A A145	0	A145
M_A A146	0	A146
M_A A147	0	A147
M_A A148	0	A148
M_A A149	0	A149
M_A A150	0	A150
M_A A151	0	A151
M_A A152	0	A152
M_A A153	0	A153
M_A A154	0	A154
M_A A155	0	A155
M_A A156	0	A156
M_A A157	0	A157
M_A A158	0	A158
M_A A159	0	A159
M_A A160	0	A160
M_A A161	0	A161
M_A A162	0	A162
M_A A163	0	A163
M_A A164	0	A164
M_A A165	0	A165
M_A A166	0	A166
M_A A167	0	A167
M_A A168	0	A168
M_A A169	0	A169
M_A A170	0	A170
M_A A171	0	A171
M_A A172	0	A172
M_A A173	0	A173
M_A A174	0	A174
M_A A175	0	A175
M_A A176	0	A176
M_A A177	0	A177
M_A A178	0	A178
M_A A179	0	A179
M_A A180	0	A180
M_A A181	0	A181
M_A A182	0	A182
M_A A183	0	A183
M_A A184	0	A184
M_A A185	0	A185
M_A A186	0	A186
M_A A187	0	A187
M_A A188	0	A188
M_A A189	0	A189
M_A A190	0	A190
M_A A191	0	A191
M_A A192	0	A192
M_A A193	0	A193
M_A A194	0	A194
M_A A195	0	A195
M_A A196	0	A196
M_A A197	0	A197
M_A A198	0	A198
M_A A199	0	A199
M_A A200	0	A200
M_A A201	0	A201
M_A A202	0	A202
M_A A203	0	A203
M_A A204	0	A204
M_A A205	0	A205
M_A A206	0	A206
M_A A207	0	A207
M_A A208	0	A208
M_A A209	0	A209
M_A A210	0	A210
M_A A211	0	A211
M_A A212	0	A212
M_A A213	0	A213
M_A A214	0	A214
M_A A215	0	A215
M_A A216	0	A216
M_A A217	0	A217
M_A A218	0	A218
M_A A219	0	A219
M_A A220	0	A220
M_A A221	0	A221
M_A A222	0	A222
M_A A223	0	A223
M_A A224	0	A224
M_A A225	0	A225
M_A A226	0	A226
M_A A227	0	A227
M_A A228	0	A228
M_A A229	0	A229
M_A A230	0	A230
M_A A231	0	A231
M_A A232	0	A232
M_A A233	0	A233
M_A A234	0	A234
M_A A235	0	A235
M_A A236	0	A236
M_A A237	0	A237
M_A A238	0	A238
M_A A239	0	A239
M_A A240	0	A240
M_A A241	0	A241
M_A A242	0	A242
M_A A243	0	A243
M_A A244	0	A244
M_A A245	0	A245
M_A A246	0	A246
M_A A247	0	A247
M_A A248	0	A248
M_A A249	0	A249
M_A A250	0	A250
M_A A251	0	A251
M_A A252	0	A252
M_A A253	0	A253
M_A A254	0	A254
M_A A255	0	A255
M_A A256	0	A256
M_A A257	0	A257
M_A A258	0	A258
M_A A259	0	A259
M_A A260	0	A260
M_A A261	0	A261
M_A A262	0	A262
M_A A263	0	A263
M_A A264	0	A264
M_A A265	0	A265
M_A A266	0	A266
M_A A267	0	A267
M_A A268	0	A268
M_A A269	0	A269
M_A A270	0	A270
M_A A271	0	A271
M_A A272	0	A272
M_A A273	0	A273
M_A A274	0	A274
M_A A275	0	A275
M_A A276	0	A276
M_A A277	0	A277
M_A A278	0	A278
M_A A279	0	A279
M_A A280	0	A280
M_A A281	0	A281
M_A A282	0	A282
M_A A283	0	A283
M_A A284	0	A284
M_A A285	0	A285
M_A A286	0	A286
M_A A287	0	A287
M_A A288	0	A288
M_A A289	0	A289
M_A A290	0	A290
M_A A291	0	A291
M_A A292	0	A292
M_A A293	0	A293
M_A A294	0	A294
M_A A295	0	A295
M_A A296	0	A296
M_A A297	0	A297
M_A A298	0	A298
M_A A299	0	A299
M_A A300	0	A300
M_A A301	0	A301
M_A A302	0	A302
M_A A303	0	A303
M_A A304	0	A304
M_A A305	0	A305
M_A A306	0	A306
M_A A307	0	A307
M_A A308	0	A308
M_A A309	0	A309
M_A A310	0	A310
M_A A311	0	A311
M_A A312	0	A312
M_A A313	0	A313
M_A A314	0	A314
M_A A315	0	A315
M_A A316	0	A316
M_A A317	0	A317
M_A A318	0	A318
M_A A319	0	A319
M_A A320	0	A320
M_A A321	0	A321
M_A A322	0	A322
M_A A323	0	A323
M_A A324	0	A324
M_A A325	0	A325
M_A A326	0	A326
M_A A327	0	A327
M_A A328	0	A328
M_A A329	0	A329
M_A A330	0	A330
M_A A331	0	A331
M_A A332	0	A332
M_A A333	0	A333
M_A A334	0	A334
M_A A335	0	A335
M_A A336	0	A336
M_A A337	0	A337
M_A A338	0	A338
M_A A339	0	A339
M_A A340	0	A340
M_A A341	0	A341
M_A A342	0	A342
M_A A343	0	A343
M_A A344	0	A344
M_A A345	0	A345
M_A A346	0	A346
M_A A347	0	A347
M_A A348	0	A348
M_A A349	0	A349
M_A A350	0	A350
M_A A351	0	A351
M_A A352	0	A352
M_A A353	0	A353
M_A A354	0	A354
M_A A355	0	A355
M_A A356	0	A356
M_A A357	0	A357
M_A A358	0	A358
M_A A359	0	A359
M_A A360	0	A360
M_A A361	0	A361
M_A A362	0	A362
M_A A363	0	A363
M_A A364	0	A364
M_A A365	0	A365
M_A A366	0	A366
M_A A367	0	A367
M_A A368	0	A368
M_A A369	0	A369
M_A A370	0	A370
M_A A371	0	A371
M_A A372	0	A372
M_A A373	0	A373
M_A A374	0	A374
M_A A375	0	A375
M_A A376	0	A376
M_A A377	0	A377
M_A A378	0	A378
M_A A379	0	A379
M_A A380	0	A380
M_A A381	0	A381
M_A A382	0	A382
M_A A383	0	A383
M_A A384	0	A384
M_A A385	0	A385
M_A A386	0	A386
M_A A387	0	A387
M_A A388	0	A388
M_A A389	0	A389
M_A A390	0	A390
M_A A391	0	A391
M_A A392	0	A392
M_A A393	0	A393
M_A A394	0	A394
M_A A395	0	A395
M_A A396	0	A396
M_A A397	0	A397
M_A A398	0	A398
M_A A399	0	A399
M_A A400	0	A40

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

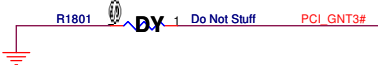
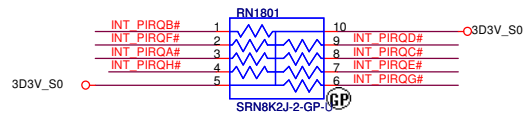
Document Number
Enrico/Caruso 15 HR

Rev
X01

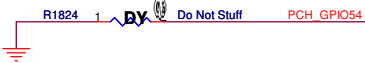
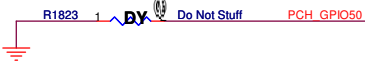
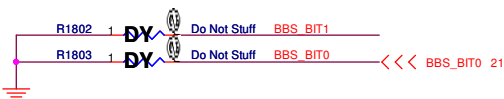
Date: Thursday, June 02, 2011

Sheet 16 of 104

SSID = PCH

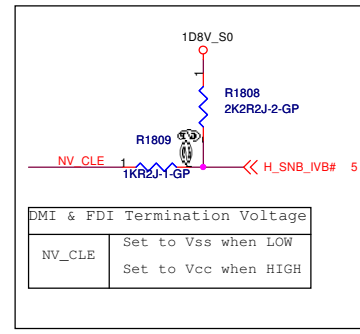
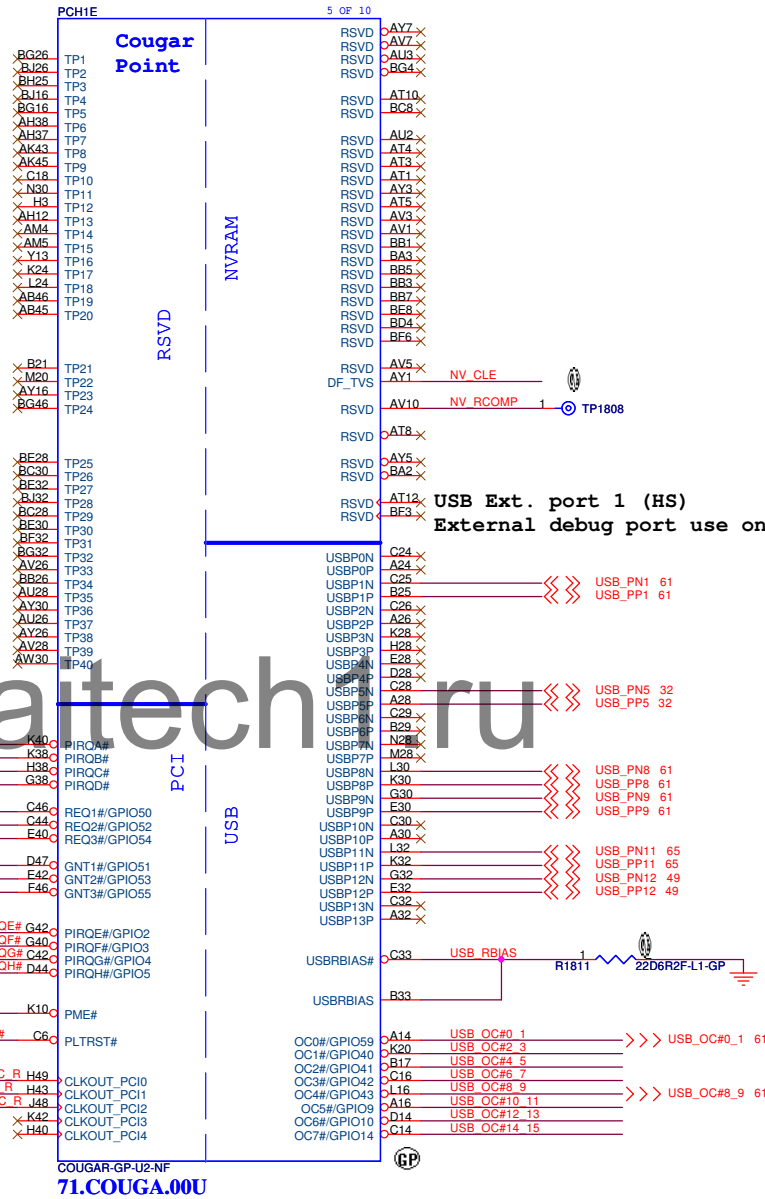
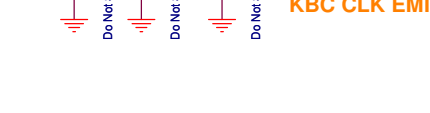
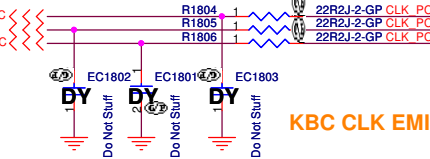


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

56 SATA_ODD_DA# >>> R1813 1 2 Do Not Stuff



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

USB Ext. port 1 (HS)
External debug port use on Huron river platform
USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Enrico/Caruso 15 HR

Rev X01

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



PCH1C

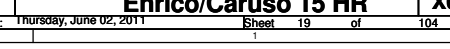
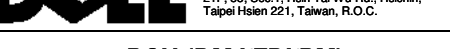
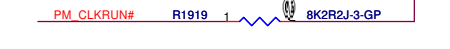
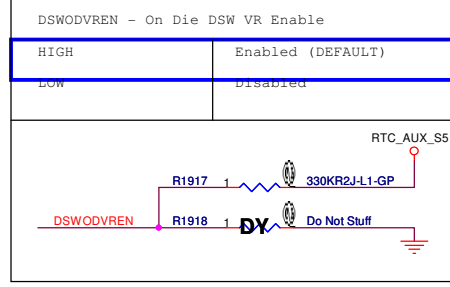
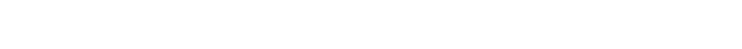
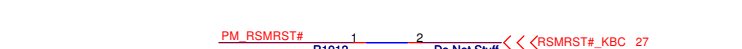
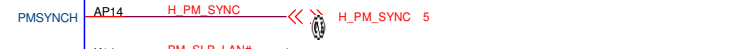
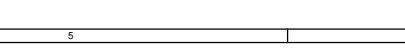
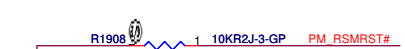
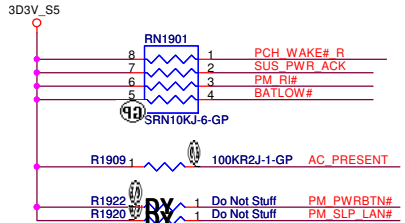
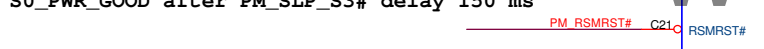
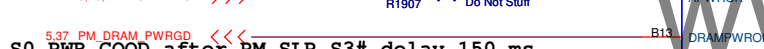
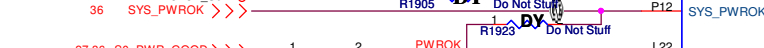
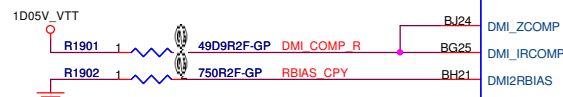
3 OF 10

Cougar Point

DMI FDI

System Power Management

COUGAR-GP-U2-NF
71.COUGA.00U



DV15 HR Vos GIGA HDMI NoSurge

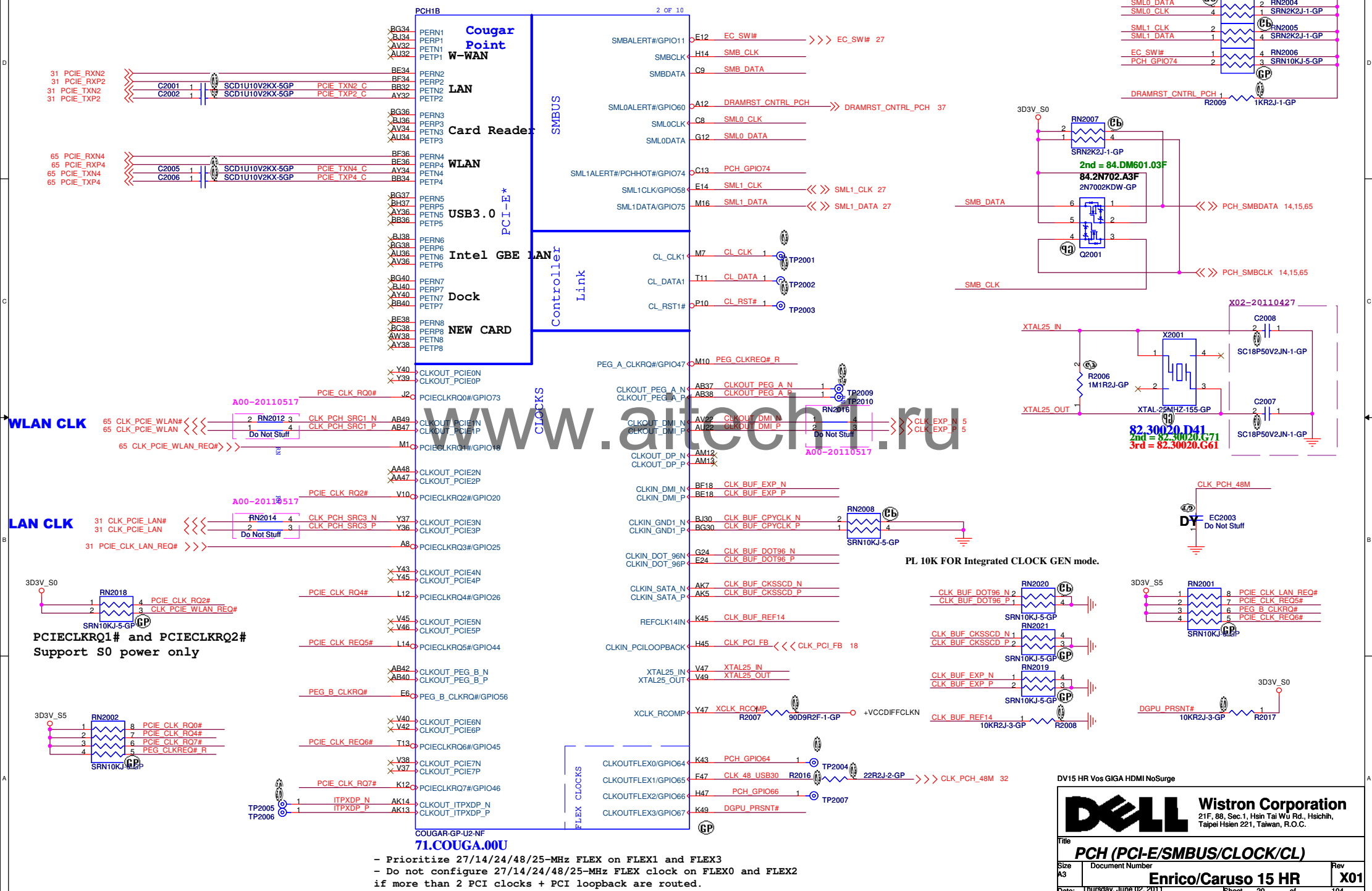
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **PCH (DM I/FDI/PM)**

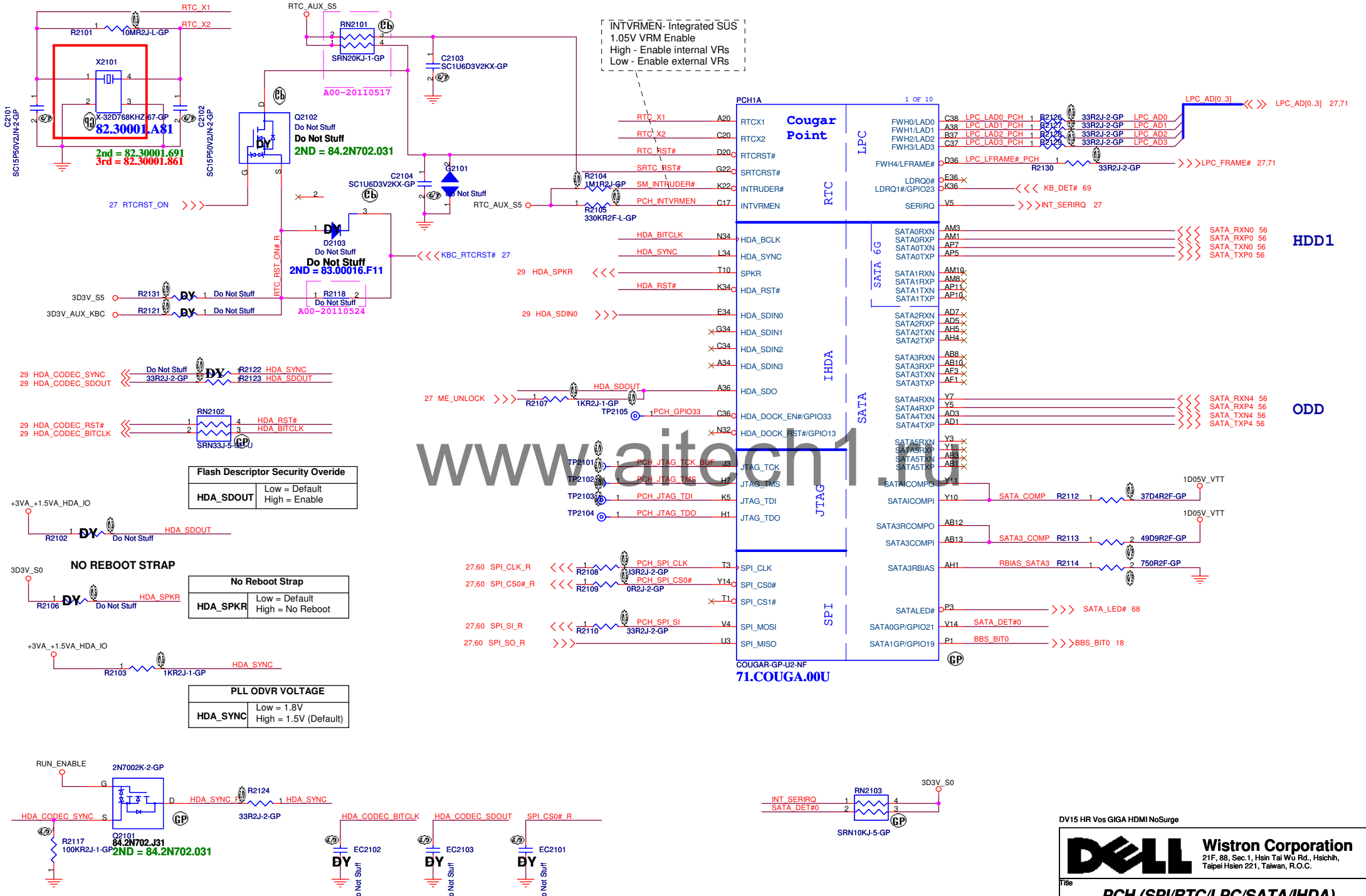
Size A3 Document Number **Enrico/Caruso 15 HR** Rev **X01**

Date: Thursday, June 02, 2011 Sheet 19 of 104

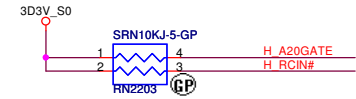
SSID = PCH



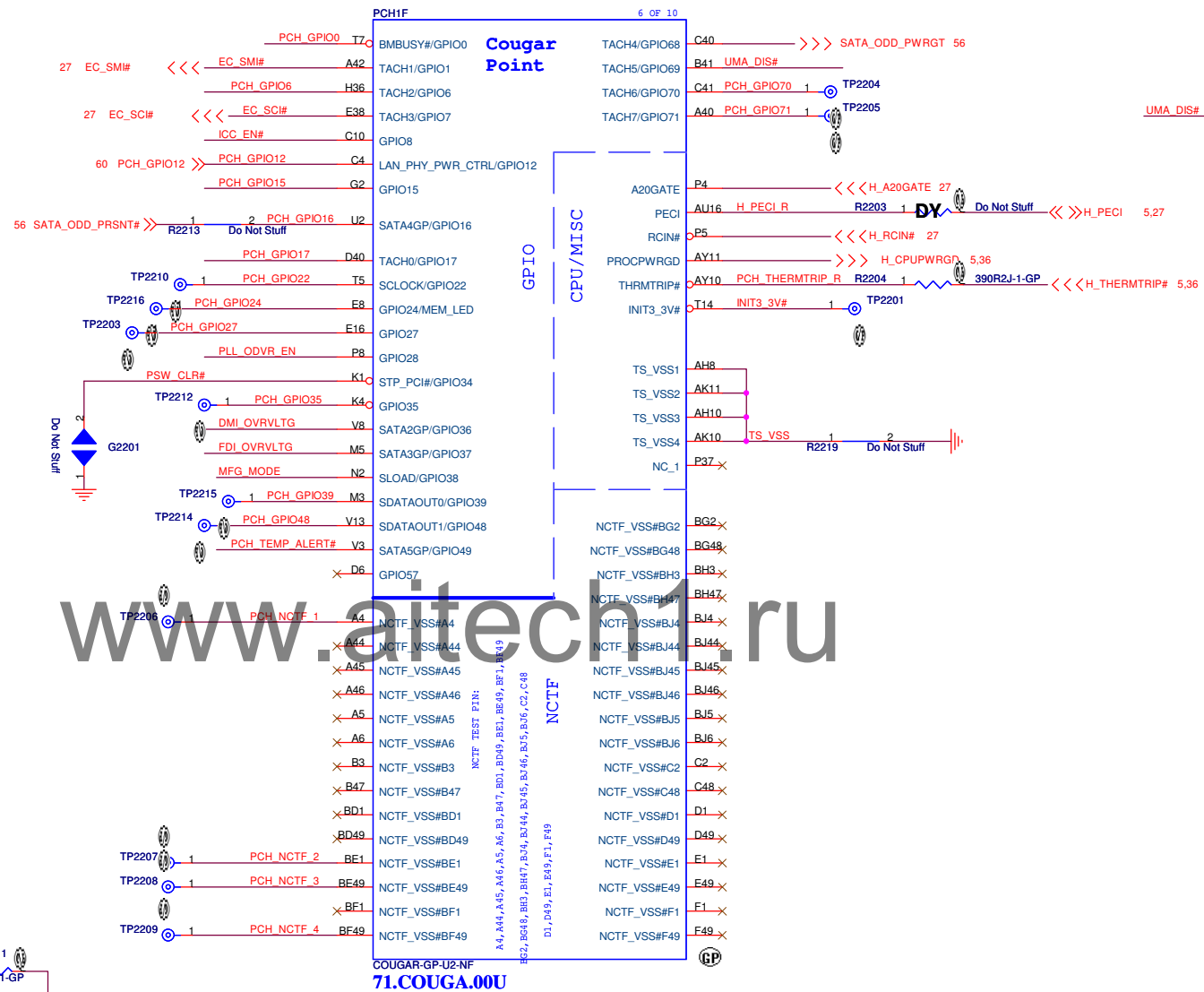
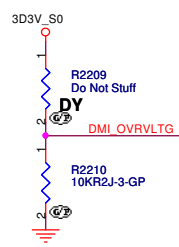
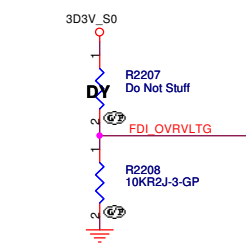
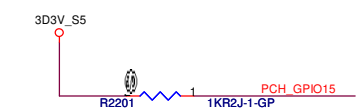
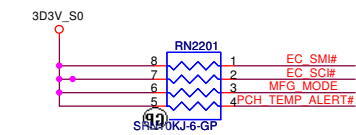
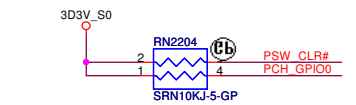
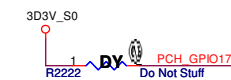
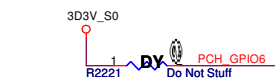
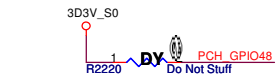
SSID = PCH



SSID = PCH

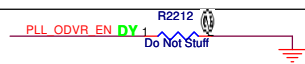


GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

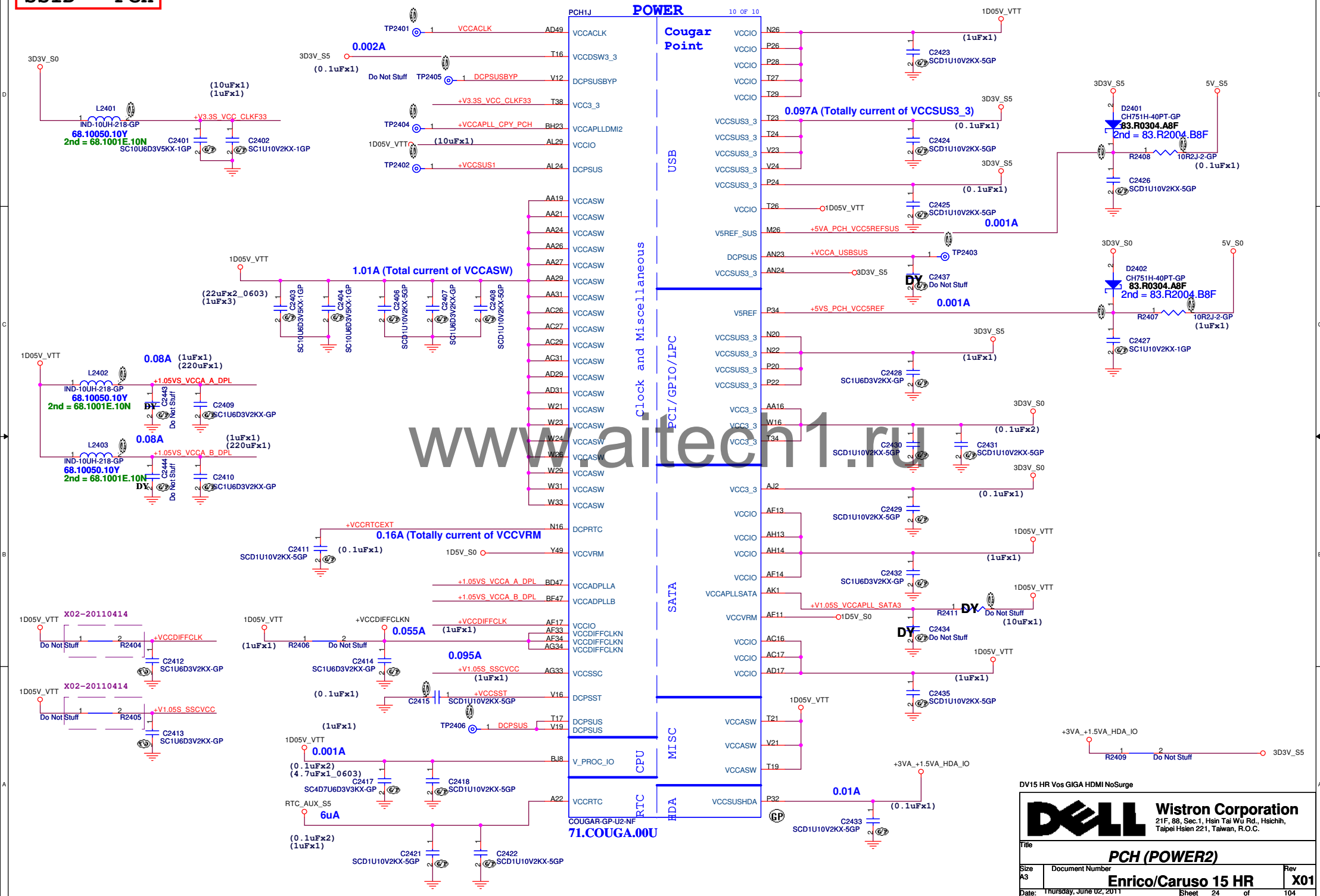


PLL ON DIE VR ENABLE

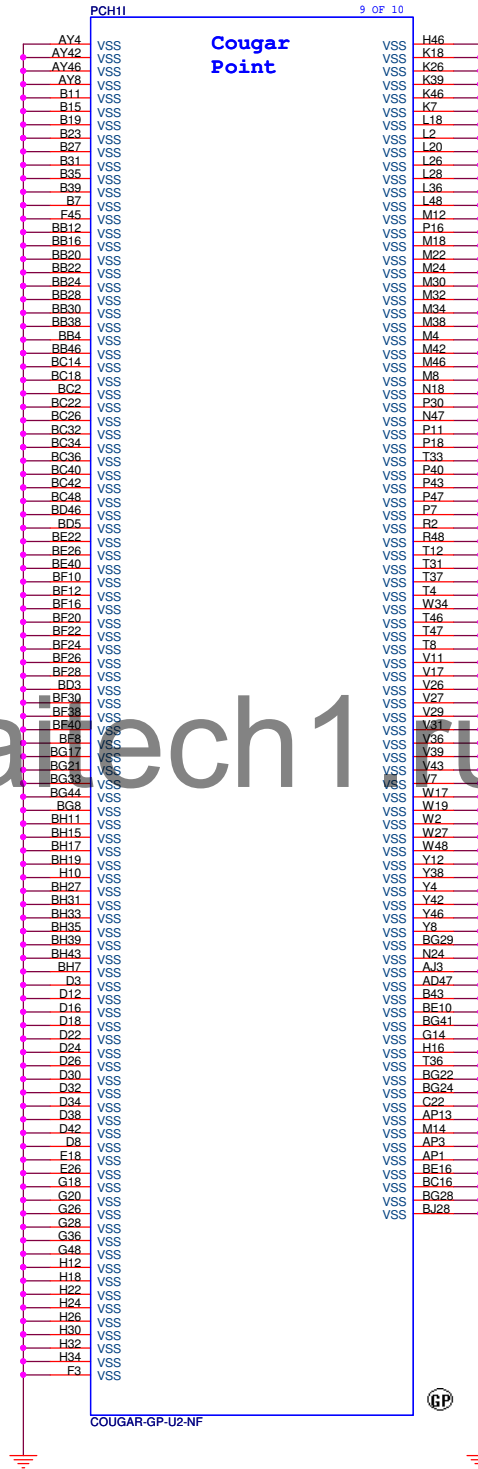
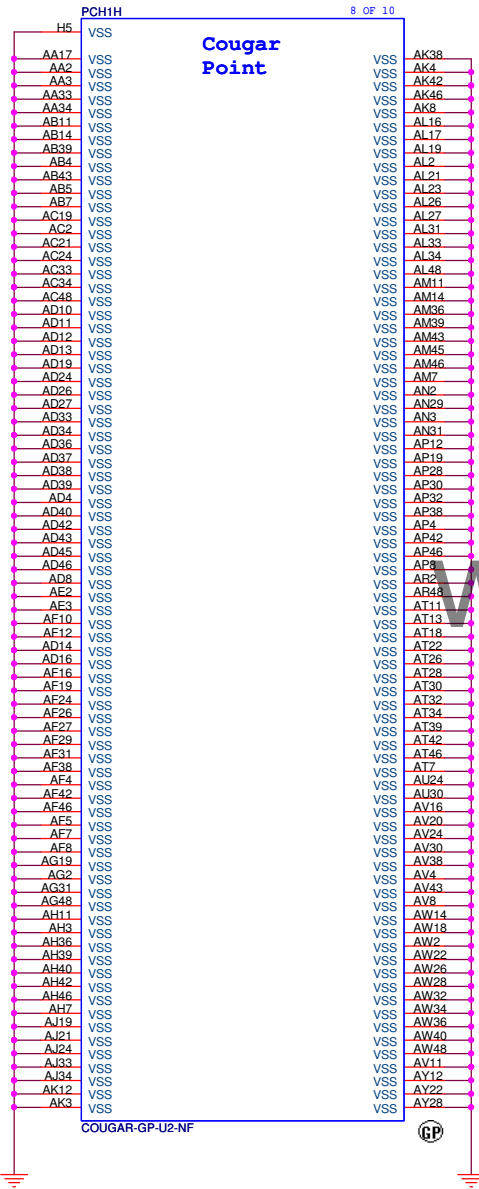
NOTE: This signal has a weak internal pull-up 20K
 ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
 DISABLED -- LOW (R2212 STUFFED)



SSID = PCH



SSID = PCH



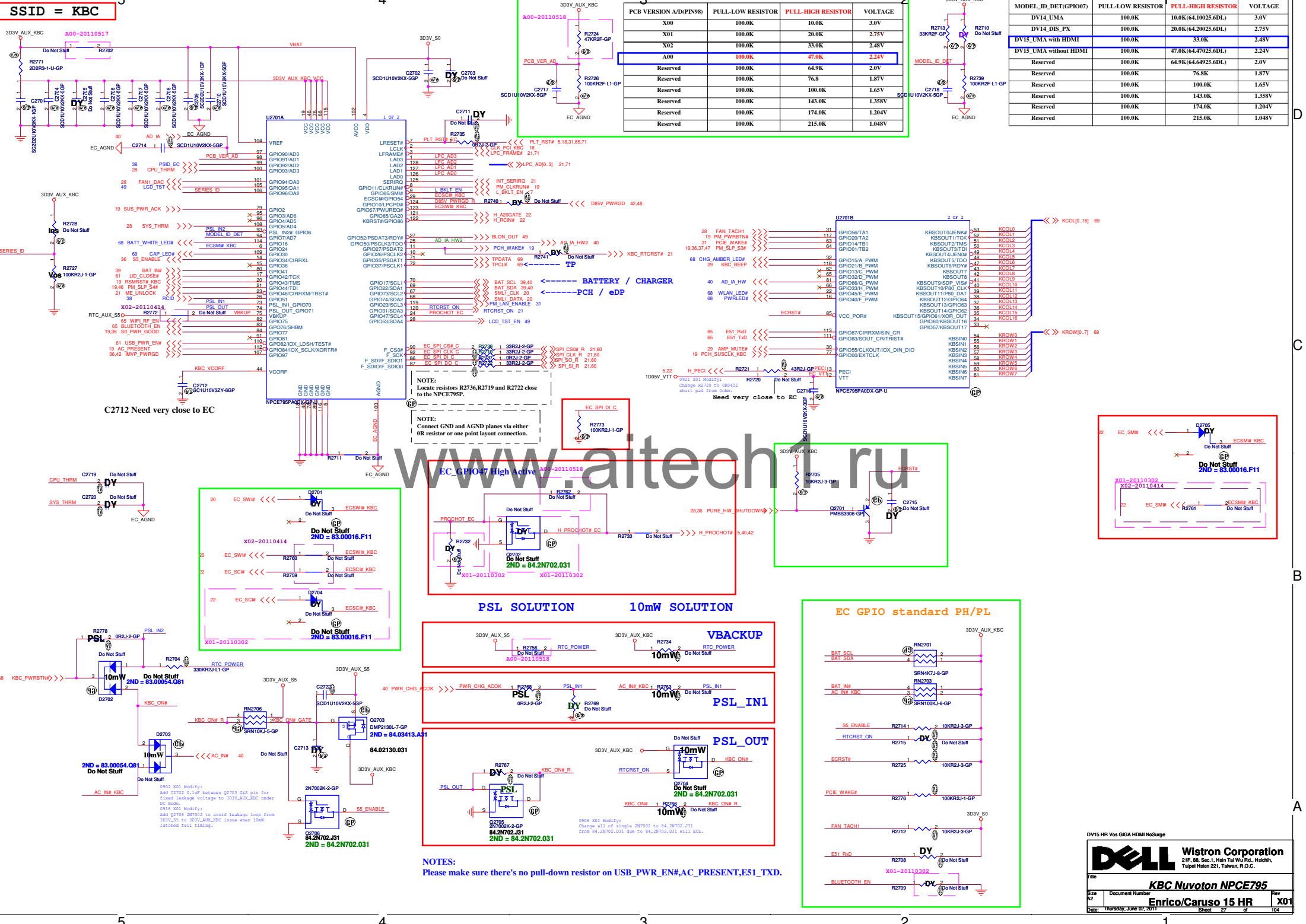
DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title PCH (VSS)		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 25	of 104

(Blanking)
www.aitech1.ru

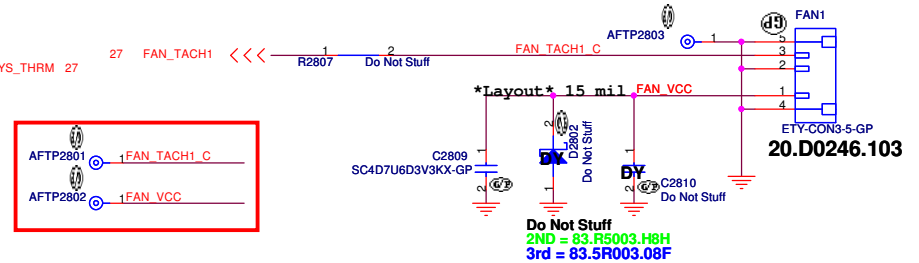
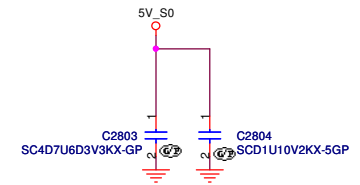
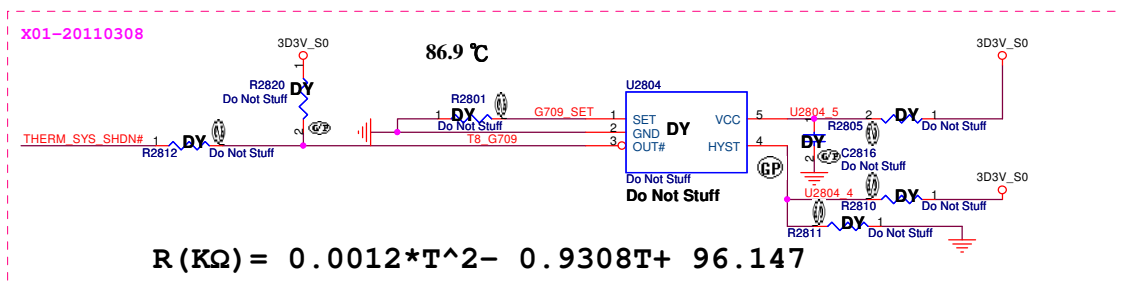
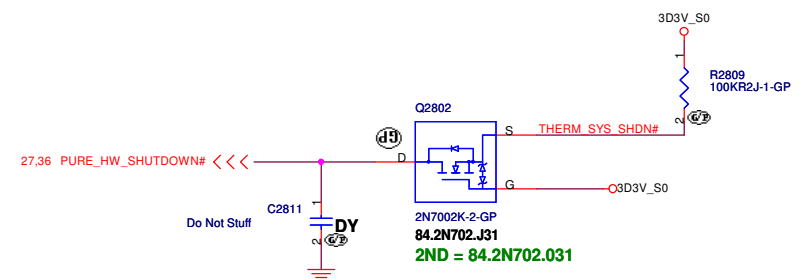
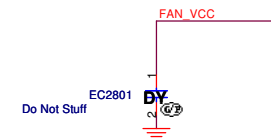


MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

GPIO	FUNCTION	VALUE
GPIO01/AD0	LCLK	100K
GPIO01/AD1	LFRAME#	100K
GPIO02/AD2	LAD0	100K
GPIO03/AD3	LAD1	100K
GPIO04/AD4	LAD0	100K
GPIO05/AD5	LAD1	100K
GPIO06/AD6	LAD0	100K
GPIO07/AD7	LAD1	100K
GPIO08/AD8	LAD0	100K
GPIO09/AD9	LAD1	100K
GPIO10/AD10	LAD0	100K
GPIO11/AD11	LAD1	100K
GPIO12/AD12	LAD0	100K
GPIO13/AD13	LAD1	100K
GPIO14/AD14	LAD0	100K
GPIO15/AD15	LAD1	100K
GPIO16/AD16	LAD0	100K
GPIO17/AD17	LAD1	100K
GPIO18/AD18	LAD0	100K
GPIO19/AD19	LAD1	100K
GPIO20/AD20	LAD0	100K
GPIO21/AD21	LAD1	100K
GPIO22/AD22	LAD0	100K
GPIO23/AD23	LAD1	100K
GPIO24/AD24	LAD0	100K
GPIO25/AD25	LAD1	100K
GPIO26/AD26	LAD0	100K
GPIO27/AD27	LAD1	100K
GPIO28/AD28	LAD0	100K
GPIO29/AD29	LAD1	100K
GPIO30/AD30	LAD0	100K
GPIO31/AD31	LAD1	100K
GPIO32/AD32	LAD0	100K
GPIO33/AD33	LAD1	100K
GPIO34/AD34	LAD0	100K
GPIO35/AD35	LAD1	100K
GPIO36/AD36	LAD0	100K
GPIO37/AD37	LAD1	100K
GPIO38/AD38	LAD0	100K
GPIO39/AD39	LAD1	100K
GPIO40/AD40	LAD0	100K
GPIO41/AD41	LAD1	100K
GPIO42/AD42	LAD0	100K
GPIO43/AD43	LAD1	100K
GPIO44/AD44	LAD0	100K
GPIO45/AD45	LAD1	100K
GPIO46/AD46	LAD0	100K
GPIO47/AD47	LAD1	100K
GPIO48/AD48	LAD0	100K
GPIO49/AD49	LAD1	100K
GPIO50/AD50	LAD0	100K
GPIO51/AD51	LAD1	100K
GPIO52/AD52	LAD0	100K
GPIO53/AD53	LAD1	100K
GPIO54/AD54	LAD0	100K
GPIO55/AD55	LAD1	100K
GPIO56/AD56	LAD0	100K
GPIO57/AD57	LAD1	100K
GPIO58/AD58	LAD0	100K
GPIO59/AD59	LAD1	100K
GPIO60/AD60	LAD0	100K
GPIO61/AD61	LAD1	100K
GPIO62/AD62	LAD0	100K
GPIO63/AD63	LAD1	100K
GPIO64/AD64	LAD0	100K
GPIO65/AD65	LAD1	100K
GPIO66/AD66	LAD0	100K
GPIO67/AD67	LAD1	100K
GPIO68/AD68	LAD0	100K
GPIO69/AD69	LAD1	100K
GPIO70/AD70	LAD0	100K
GPIO71/AD71	LAD1	100K
GPIO72/AD72	LAD0	100K
GPIO73/AD73	LAD1	100K
GPIO74/AD74	LAD0	100K
GPIO75/AD75	LAD1	100K
GPIO76/AD76	LAD0	100K
GPIO77/AD77	LAD1	100K
GPIO78/AD78	LAD0	100K
GPIO79/AD79	LAD1	100K
GPIO80/AD80	LAD0	100K
GPIO81/AD81	LAD1	100K
GPIO82/AD82	LAD0	100K
GPIO83/AD83	LAD1	100K
GPIO84/AD84	LAD0	100K
GPIO85/AD85	LAD1	100K
GPIO86/AD86	LAD0	100K
GPIO87/AD87	LAD1	100K
GPIO88/AD88	LAD0	100K
GPIO89/AD89	LAD1	100K
GPIO90/AD90	LAD0	100K
GPIO91/AD91	LAD1	100K
GPIO92/AD92	LAD0	100K
GPIO93/AD93	LAD1	100K
GPIO94/AD94	LAD0	100K
GPIO95/AD95	LAD1	100K
GPIO96/AD96	LAD0	100K
GPIO97/AD97	LAD1	100K
GPIO98/AD98	LAD0	100K
GPIO99/AD99	LAD1	100K
GPIO100/AD100	LAD0	100K
GPIO101/AD101	LAD1	100K
GPIO102/AD102	LAD0	100K
GPIO103/AD103	LAD1	100K
GPIO104/AD104	LAD0	100K
GPIO105/AD105	LAD1	100K
GPIO106/AD106	LAD0	100K
GPIO107/AD107	LAD1	100K
GPIO108/AD108	LAD0	100K
GPIO109/AD109	LAD1	100K
GPIO110/AD110	LAD0	100K
GPIO111/AD111	LAD1	100K
GPIO112/AD112	LAD0	100K
GPIO113/AD113	LAD1	100K
GPIO114/AD114	LAD0	100K
GPIO115/AD115	LAD1	100K
GPIO116/AD116	LAD0	100K
GPIO117/AD117	LAD1	100K
GPIO118/AD118	LAD0	100K
GPIO119/AD119	LAD1	100K
GPIO120/AD120	LAD0	100K
GPIO121/AD121	LAD1	100K
GPIO122/AD122	LAD0	100K
GPIO123/AD123	LAD1	100K
GPIO124/AD124	LAD0	100K
GPIO125/AD125	LAD1	100K
GPIO126/AD126	LAD0	100K
GPIO127/AD127	LAD1	100K
GPIO128/AD128	LAD0	100K
GPIO129/AD129	LAD1	100K
GPIO130/AD130	LAD0	100K
GPIO131/AD131	LAD1	100K
GPIO132/AD132	LAD0	100K
GPIO133/AD133	LAD1	100K
GPIO134/AD134	LAD0	100K
GPIO135/AD135	LAD1	100K
GPIO136/AD136	LAD0	100K
GPIO137/AD137	LAD1	100K
GPIO138/AD138	LAD0	100K
GPIO139/AD139	LAD1	100K
GPIO140/AD140	LAD0	100K
GPIO141/AD141	LAD1	100K
GPIO142/AD142	LAD0	100K
GPIO143/AD143	LAD1	100K
GPIO144/AD144	LAD0	100K
GPIO145/AD145	LAD1	100K
GPIO146/AD146	LAD0	100K
GPIO147/AD147	LAD1	100K
GPIO148/AD148	LAD0	100K
GPIO149/AD149	LAD1	100K
GPIO150/AD150	LAD0	100K
GPIO151/AD151	LAD1	100K
GPIO152/AD152	LAD0	100K
GPIO153/AD153	LAD1	100K
GPIO154/AD154	LAD0	100K
GPIO155/AD155	LAD1	100K
GPIO156/AD156	LAD0	100K
GPIO157/AD157	LAD1	100K
GPIO158/AD158	LAD0	100K
GPIO159/AD159	LAD1	100K
GPIO160/AD160	LAD0	100K
GPIO161/AD161	LAD1	100K
GPIO162/AD162	LAD0	100K
GPIO163/AD163	LAD1	100K
GPIO164/AD164	LAD0	100K
GPIO165/AD165	LAD1	100K
GPIO166/AD166	LAD0	100K
GPIO167/AD167	LAD1	100K
GPIO168/AD168	LAD0	100K
GPIO169/AD169	LAD1	100K
GPIO170/AD170	LAD0	100K
GPIO171/AD171	LAD1	100K
GPIO172/AD172	LAD0	100K
GPIO173/AD173	LAD1	100K
GPIO174/AD174	LAD0	100K
GPIO175/AD175	LAD1	100K
GPIO176/AD176	LAD0	100K
GPIO177/AD177	LAD1	100K
GPIO178/AD178	LAD0	100K
GPIO179/AD179	LAD1	100K
GPIO180/AD180	LAD0	100K
GPIO181/AD181	LAD1	100K
GPIO182/AD182	LAD0	100K
GPIO183/AD183	LAD1	100K
GPIO184/AD184	LAD0	100K
GPIO185/AD185	LAD1	100K
GPIO186/AD186	LAD0	100K
GPIO187/AD187	LAD1	100K
GPIO188/AD188	LAD0	100K
GPIO189/AD189	LAD1	100K
GPIO190/AD190	LAD0	100K
GPIO191/AD191	LAD1	100K
GPIO192/AD192	LAD0	100K
GPIO193/AD193	LAD1	100K
GPIO194/AD194	LAD0	100K
GPIO195/AD195	LAD1	100K
GPIO196/AD196	LAD0	100K
GPIO197/AD197	LAD1	100K
GPIO198/AD198	LAD0	100K
GPIO199/AD199	LAD1	100K
GPIO200/AD200	LAD0	100K
GPIO201/AD201	LAD1	100K
GPIO202/AD202	LAD0	100K
GPIO203/AD203	LAD1	100K
GPIO204/AD204	LAD0	100K
GPIO205/AD205	LAD1	100K
GPIO206/AD206	LAD0	100K
GPIO207/AD207	LAD1	100K
GPIO208/AD208	LAD0	100K
GPIO209/AD209	LAD1	100K
GPIO210/AD210	LAD0	100K
GPIO211/AD211	LAD1	100K
GPIO212/AD212	LAD0	100K
GPIO213/AD213	LAD1	100K
GPIO214/AD214	LAD0	100K
GPIO215/AD215	LAD1	100K
GPIO216/AD216	LAD0	100K
GPIO217/AD217	LAD1	100K
GPIO218/AD218	LAD0	100K
GPIO219/AD219	LAD1	100K
GPIO220/AD220	LAD0	100K
GPIO221/AD221	LAD1	100K
GPIO222/AD222	LAD0	100K
GPIO223/AD223	LAD1	100K
GPIO224/AD224	LAD0	100K
GPIO225/AD225	LAD1	100K
GPIO226/AD226	LAD0	100K
GPIO227/AD227	LAD1	100K
GPIO228/AD228	LAD0	100K
GPIO229/AD229	LAD1	100K
GPIO230/AD230	LAD0	100K
GPIO231/AD231	LAD1	100K
GPIO232/AD232	LAD0	100K
GPIO233/AD233	LAD1	100K
GPIO234/AD234	LAD0	100K
GPIO235/AD235	LAD1	100K
GPIO236/AD236	LAD0	100K
GPIO237/AD237	LAD1	100K
GPIO238/AD238	LAD0	100K
GPIO239/AD239	LAD1	100K
GPIO240/AD240	LAD0	100K
GPIO241/AD241	LAD1	100K
GPIO242/AD242	LAD0	100K
GPIO243/AD243	LAD1	100K
GPIO244/AD244	LAD0	100K
GPIO245/AD245	LAD1	100K
GPIO246/AD246	LAD0	100K
GPIO247/AD247	LAD1	100K
GPIO248/AD248	LAD0	100K
GPIO249/AD249	LAD1	100K
GPIO250/AD250	LAD0	100K
GPIO251/AD251	LAD1	100K
GPIO252/AD252	LAD0	100K
GPIO253/AD253	LAD1	100K
GPIO254/AD254	LAD0	100K
GPIO255/AD255	LAD1	100K
GPIO256/AD256	LAD0	100K
GPIO257/AD257	LAD1	100K
GPIO258/AD258	LAD0	100K
GPIO259/AD259	LAD1	100K
GPIO260/AD260	LAD0	100K
GPIO261/AD261	LAD1	100K
GPIO262/AD262	LAD0	100K
GPIO263/AD263	LAD1	100K
GPIO264/AD264	LAD0	100K
GPIO265/AD265	LAD1	100K
GPIO266/AD266	LAD0	100K
GPIO267/AD267	LAD1	100K
GPIO268/AD268	LAD0	100K
GPIO269/AD269	LAD1	100K
GPIO270/AD270	LAD0	100K
GPIO271/AD271	LAD1	100K
GPIO272/AD272	LAD0	100K
GPIO273/AD273	LAD1	100K
GPIO274/AD274	LAD0	100K
GPIO275/AD275	LAD1	100K
GPIO276/AD276	LAD0	100K
GPIO277/AD277	LAD1	100K
GPIO278/AD278	LAD0	100K
GPIO279/AD279	LAD1	100K
GPIO280/AD280	LAD0	100K
GPIO281/AD281	LAD1	100K
GPIO282/AD282	LAD0	100K
GPIO283/AD283	LAD1	100K
GPIO284/AD284	LAD0	100K
GPIO285/AD285	LAD1	100K
GPIO286/AD286	LAD0	100K
GPIO287/AD287	LAD1	100K
GPIO288/AD288	LAD0	100K
GPIO289/AD289	LAD1	100K
GPIO290/AD290	LAD0	100K
GPIO291/AD291	LAD1	100K
GPIO292/AD292	LAD0	100K
GPIO293/AD293	LAD1	100K
GPIO294/AD294	LAD0	100K
GPIO295/AD295	LAD1	100K
GPIO296/AD296	LAD0	100K
GPIO297/AD297	LAD1	100K
GPIO298/AD298	LAD0	100K
GPIO299/AD299	LAD1	100K
GPIO300/AD300	LAD0	100K
GPIO301/AD301	LAD1	100K
GPIO302/AD302	LAD0	100K
GPIO303/AD303	LAD1	100K
GPIO304/AD304	LAD0	100K
GPIO305/AD305	LAD1	100K
GPIO306/AD306	LAD0	100K
GPIO307/AD307	LAD1	100K
GPIO308/AD308	LAD0	100K
GPIO309/AD309	LAD1	100K
GPIO310/AD310	LAD0	100K
GPIO311/AD311	LAD1	100K
GPIO312/AD312	LAD0	100K
GPIO313/AD313	LAD1	100K
GPIO314/AD314	LAD0	100K
GPIO315/AD315	LAD1	100K
GPIO316/AD316	LAD0	100K
GPIO317/AD317	LAD1	100K
GPIO318/AD318	LAD0	100K
GPIO319/AD319	LAD1	100K
GPIO320/AD320	LAD0	100K
GPIO321/AD321	LAD1	100K
GPIO322/AD322	LAD0	100K
GPIO323/AD323	LAD1	100K
GPIO324/AD324	LAD0	100K
GPIO325/AD325	LAD1	100K
GPIO326/AD326	LAD0	100K
GPIO327/AD327	LAD1	100K
GPIO328/AD328	LAD0	100K
GPIO329/AD329	LAD1	100K
GPIO330/AD330	LAD0	100K
GPIO331/AD331	LAD1	100K
GPIO332/AD332	LAD0	100K
GPIO333/AD333		

Thermal sensor P2800

**EMI/ESD**

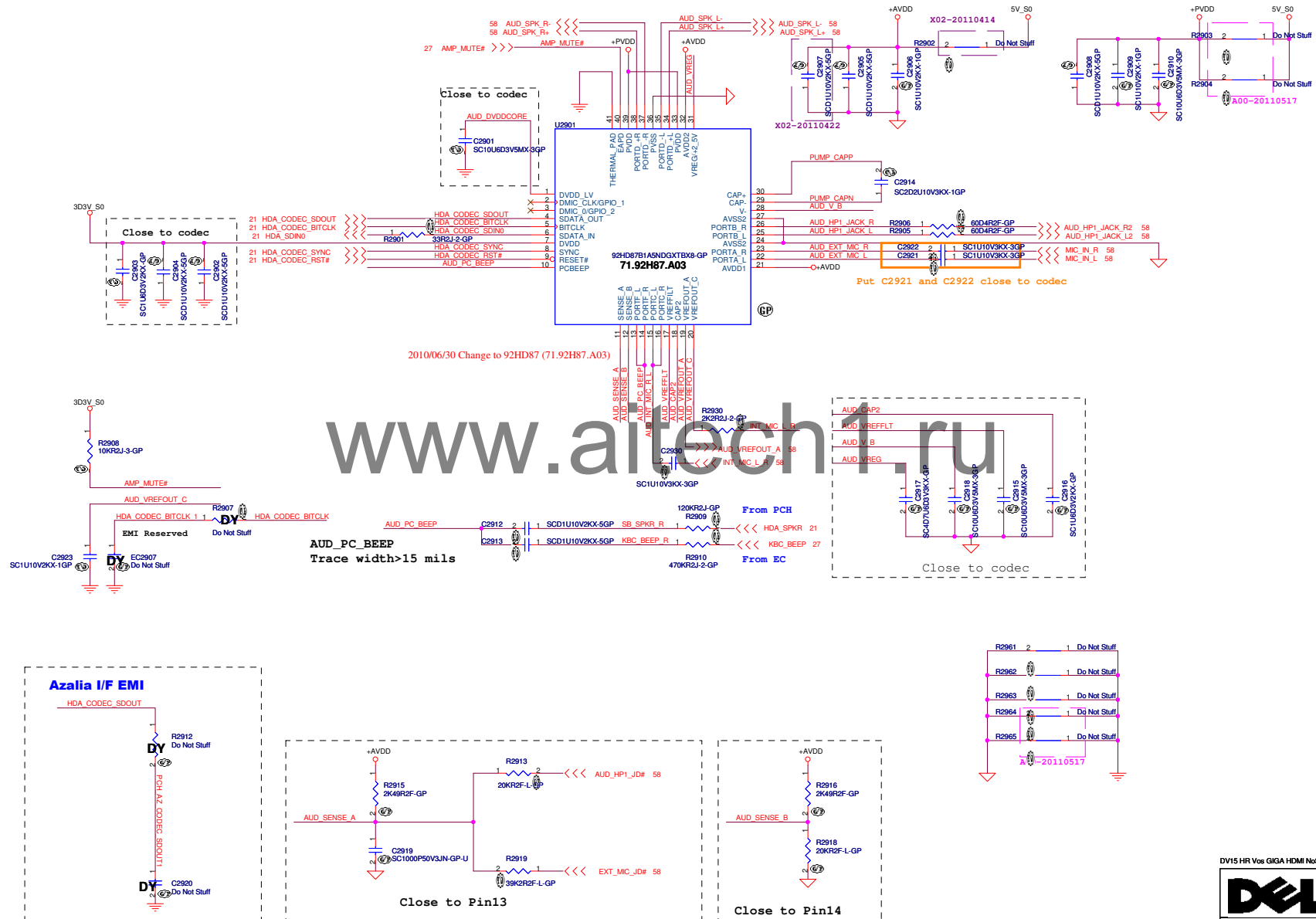
DV15 HR Vos GIGA HDMI NoSurge

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title Thermal P2800/Fan Controllor P2793			
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01	
Date: Thursday, June 02, 2011	Sheet 28 of 104		

SSID = AUDIO

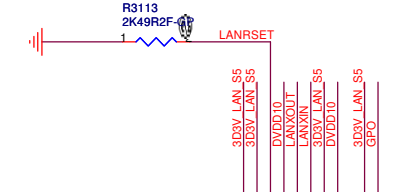
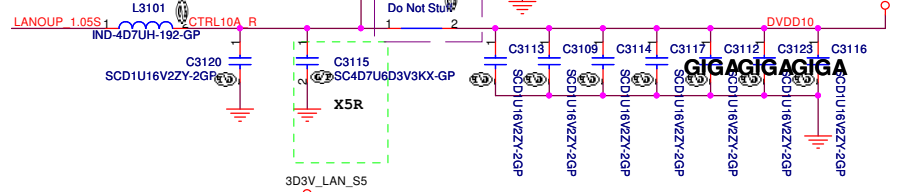


www.aitech1.ru

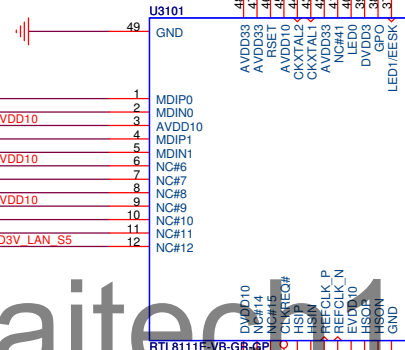
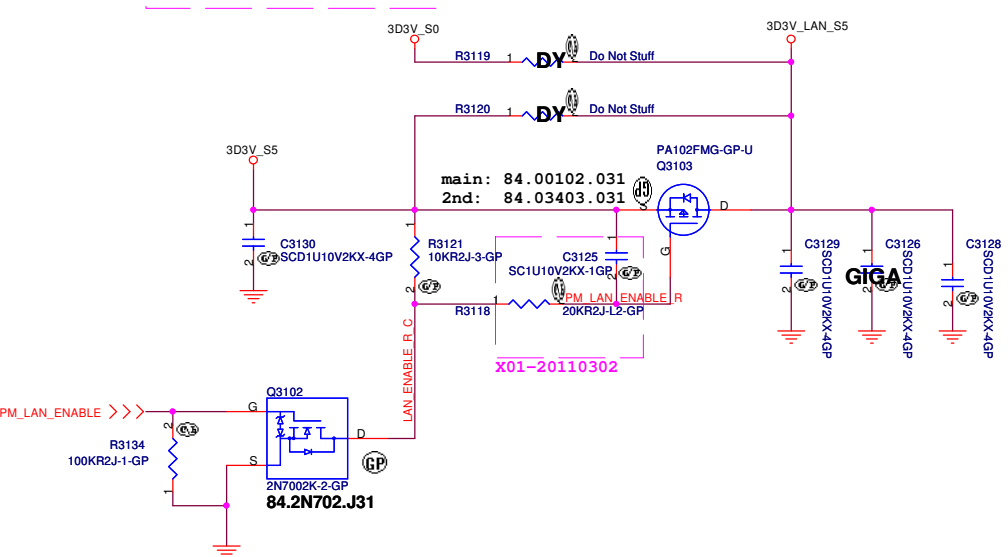
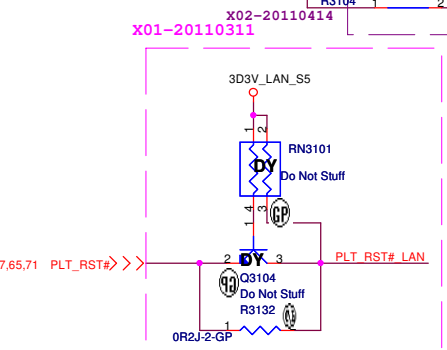
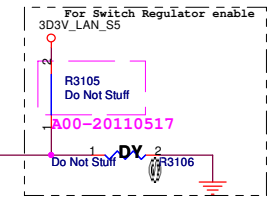
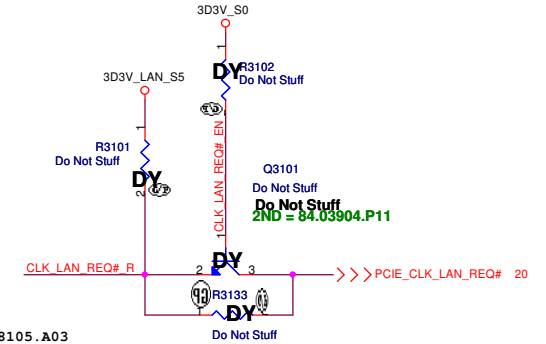
LAN CHIP

60 mils

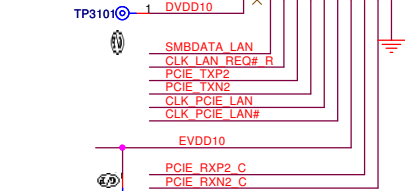
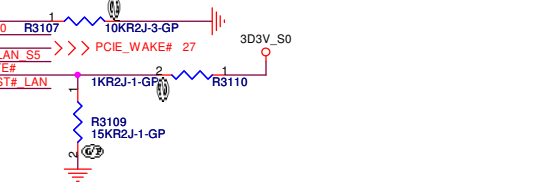
40 mils



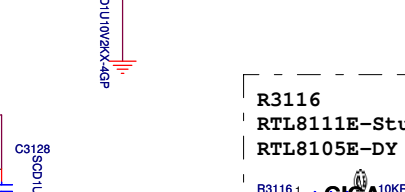
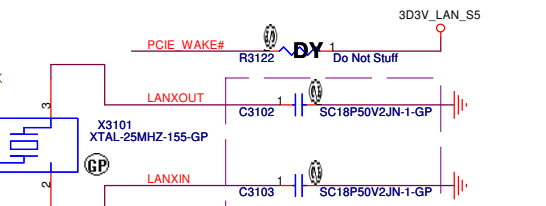
RTL8105E P/N: 71.08105.A03
RTL8111E P/N: 71.08111.I03



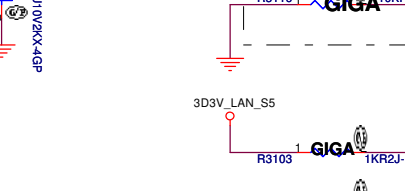
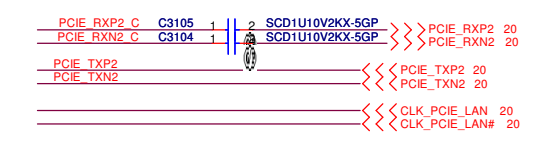
REGOUT
VDDREG
VDDREG
ENSWREG
EEDI
LED3/EEDO
EECS
DVDD10
LANWAKE#
DVDD33
ISOLATE#
PLT_RST# LAN



PCIE_WAKE#
LANXOUT
LANXIN
PCIE_RXP2_C
PCIE_RXN2_C
PCIE_TXP2
PCIE_TXN2
CLK_PCIE_LAN
CLK_PCIE_LAN#



PCIE_RXP2_C
PCIE_RXN2_C
PCIE_TXP2
PCIE_TXN2
CLK_PCIE_LAN
CLK_PCIE_LAN#



PCIE_RXP2_C
PCIE_RXN2_C
PCIE_TXP2
PCIE_TXN2
CLK_PCIE_LAN
CLK_PCIE_LAN#



PCIE_RXP2_C
PCIE_RXN2_C
PCIE_TXP2
PCIE_TXN2
CLK_PCIE_LAN
CLK_PCIE_LAN#



DV15 HR Vos GIGA HDMI NoSurge

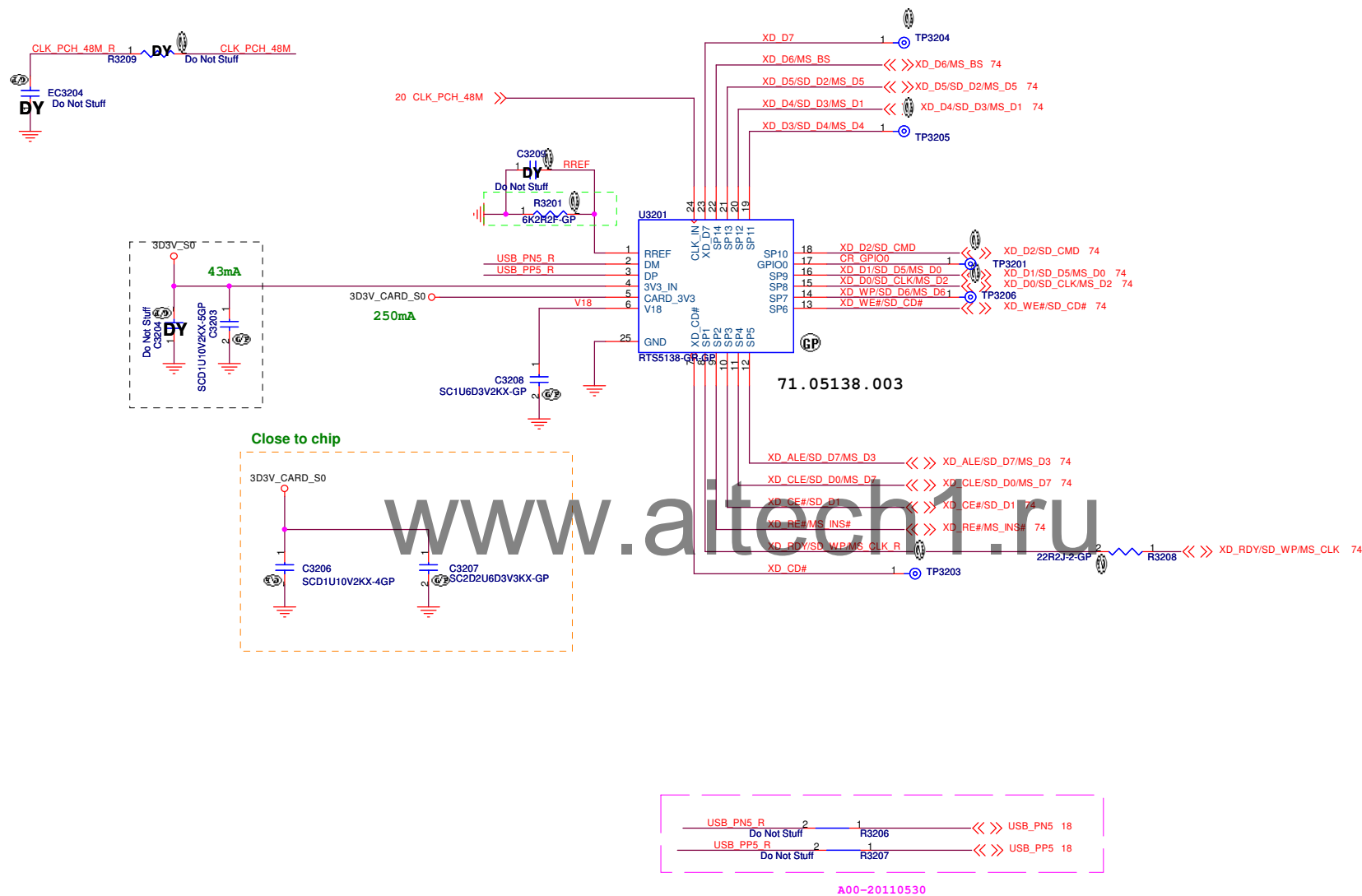
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LOM**

Size: A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet: 31 of 104

SSID = SDIO



A00-20110530

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5138

Size
A3

Document Number

Enrico/Caruso 15 HR

Date: Thursday, June 02, 2011

Sheet 32 of 104

(Blanking)

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
...

Reserved

Size	A3
------	----

Document Number

Enrico/Caruso 15 HR

Rev

X01

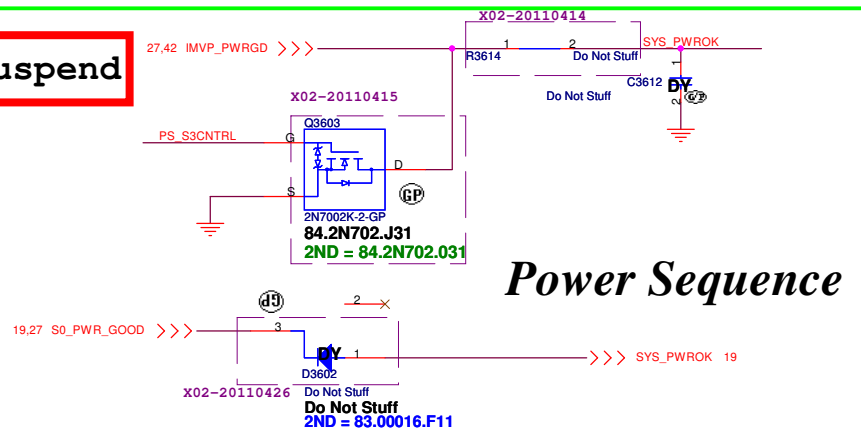
Date: Thursday, June 02, 2011

Sheet	33	of	104
-------	----	----	-----

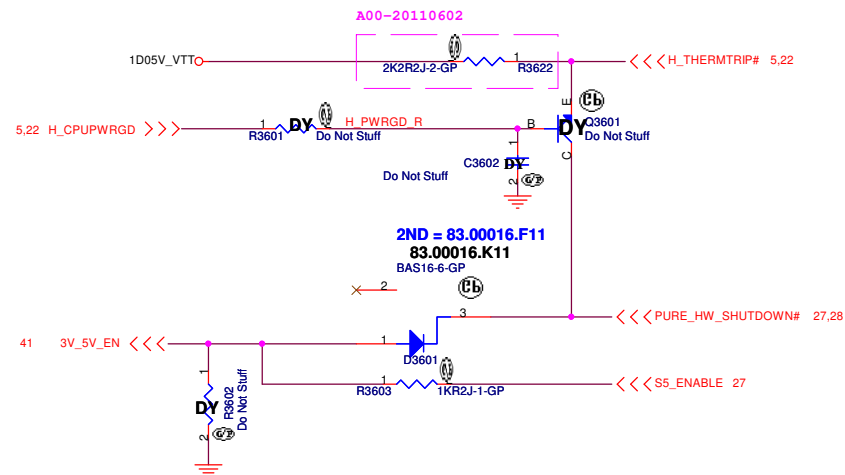
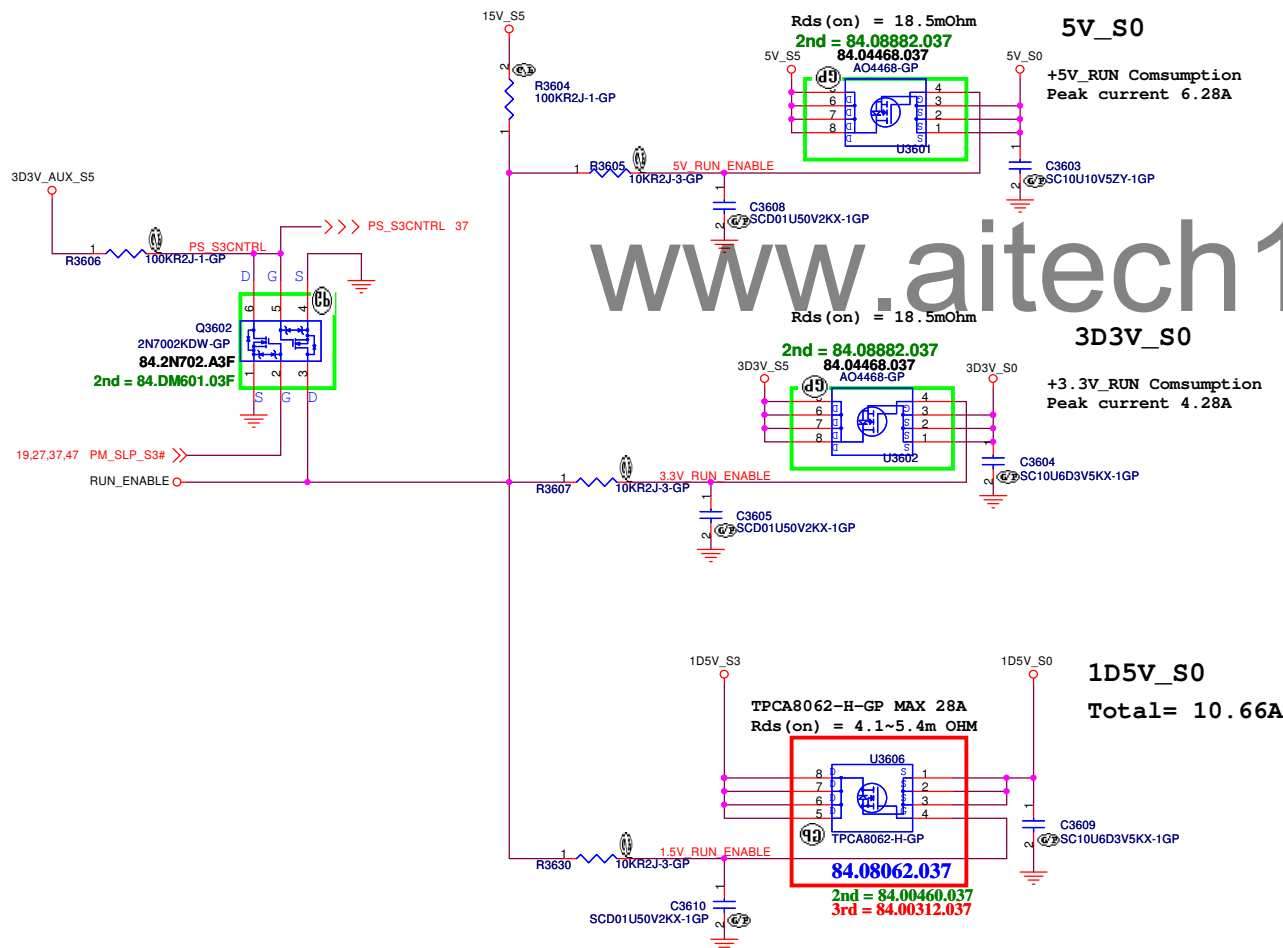
www.aitech1.ru

www.aitech1.ru

SSID = Reset.Suspend



ROSA Run Power



www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



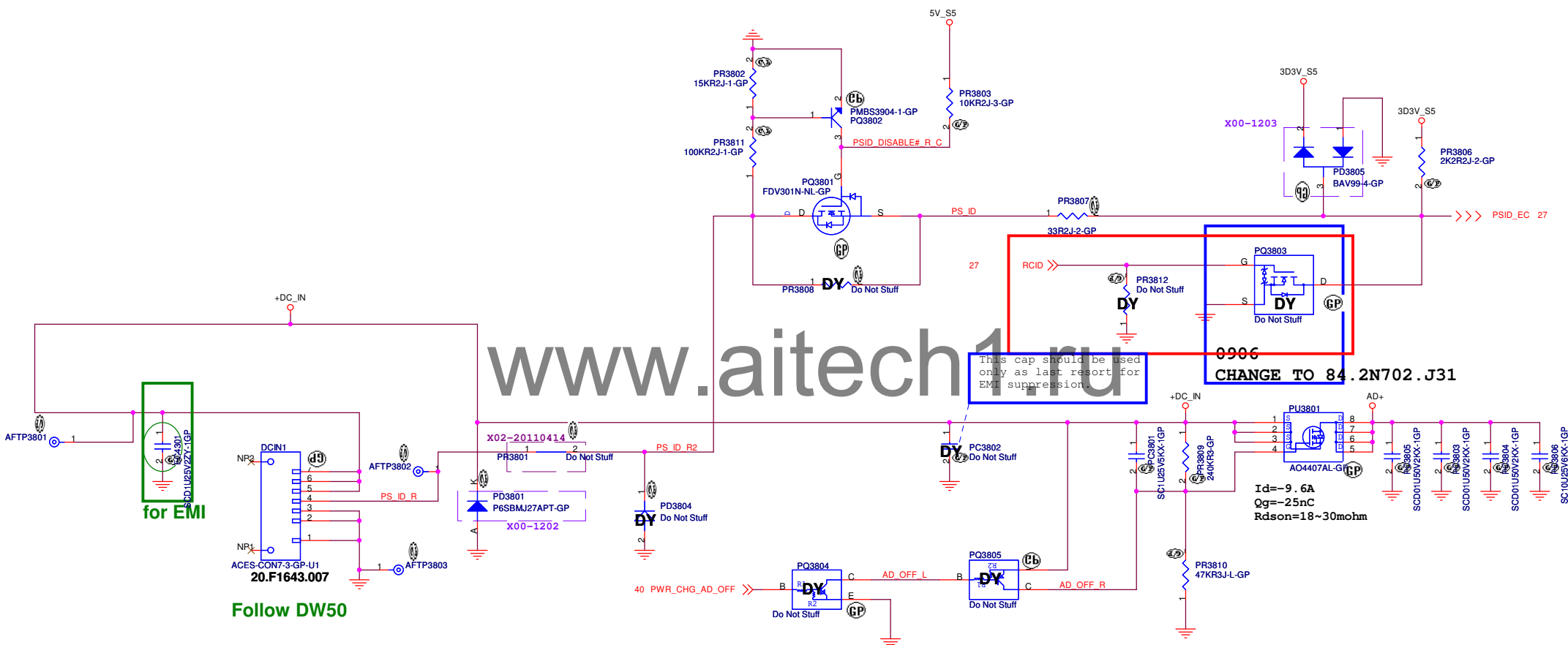
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Power Plane Enable	
Size	Document Number		Rev	
A3			Enrico/Caruso 15 HR	
Date:	Thursday, June 02, 2011	Sheet	36	of 104

X01

SSID = PWR.Support

DCin CONN

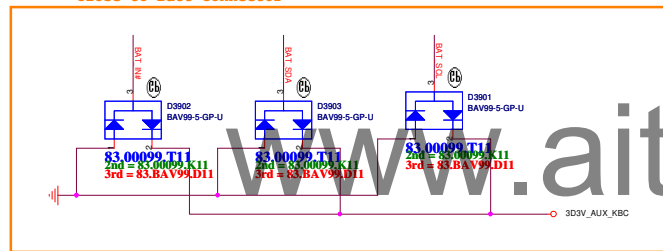
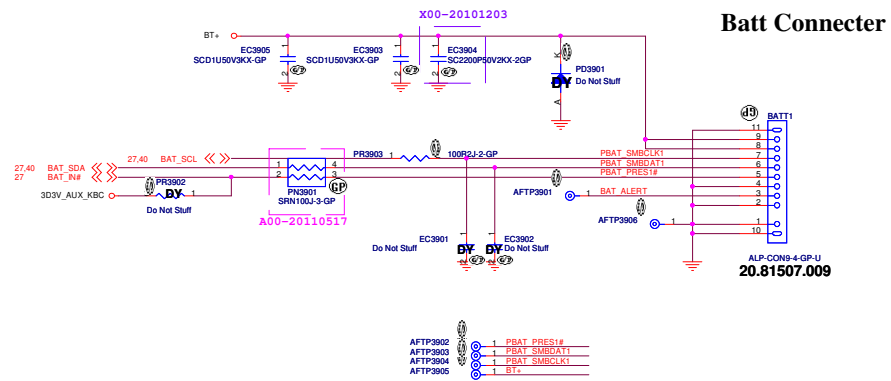


DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DCIN	
Size	Document Number	Rev		
A3	Enrico/Caruso 15 HR	X01		
Date: Thursday, June 02, 2011		Sheet	38	of 104



DV15 HR Vos GIGA HDMI NoSurge

SSID = Charger

EE need pull high and net name

0802 Rename H_PROCHOT#

27,42 H_PROCHOT#

PWR_CHG_CMPIN

PR4029 54K9R2F-L-GP

PQ4004 2N7002A-7-GP

CHG_AGIN

AD_IA_HW 27

CHG_AGIN

PWR_CHG_CMPIN

PR4027 19K6R2F-GP

PQ4003 2N7002A-7-GP

CHG_AGIN

CHG_AGIN

AD_IA_HW2 27

CHG_AGIN

AD_IA_HW 27

CHG_AGIN

CHG_AGIN

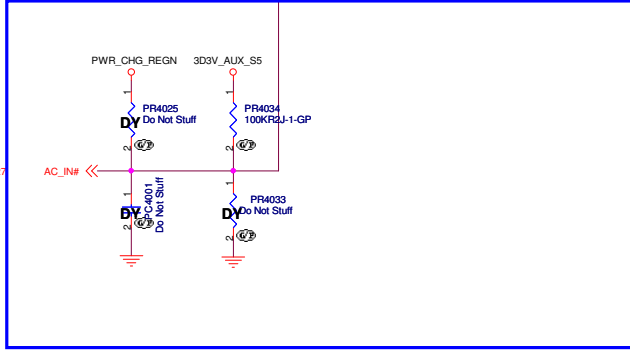
ROSA

Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

EE need check pull high



Charger Current=1.4~3.6A

DV15 HR Vos GIGA HDMI NoSurge

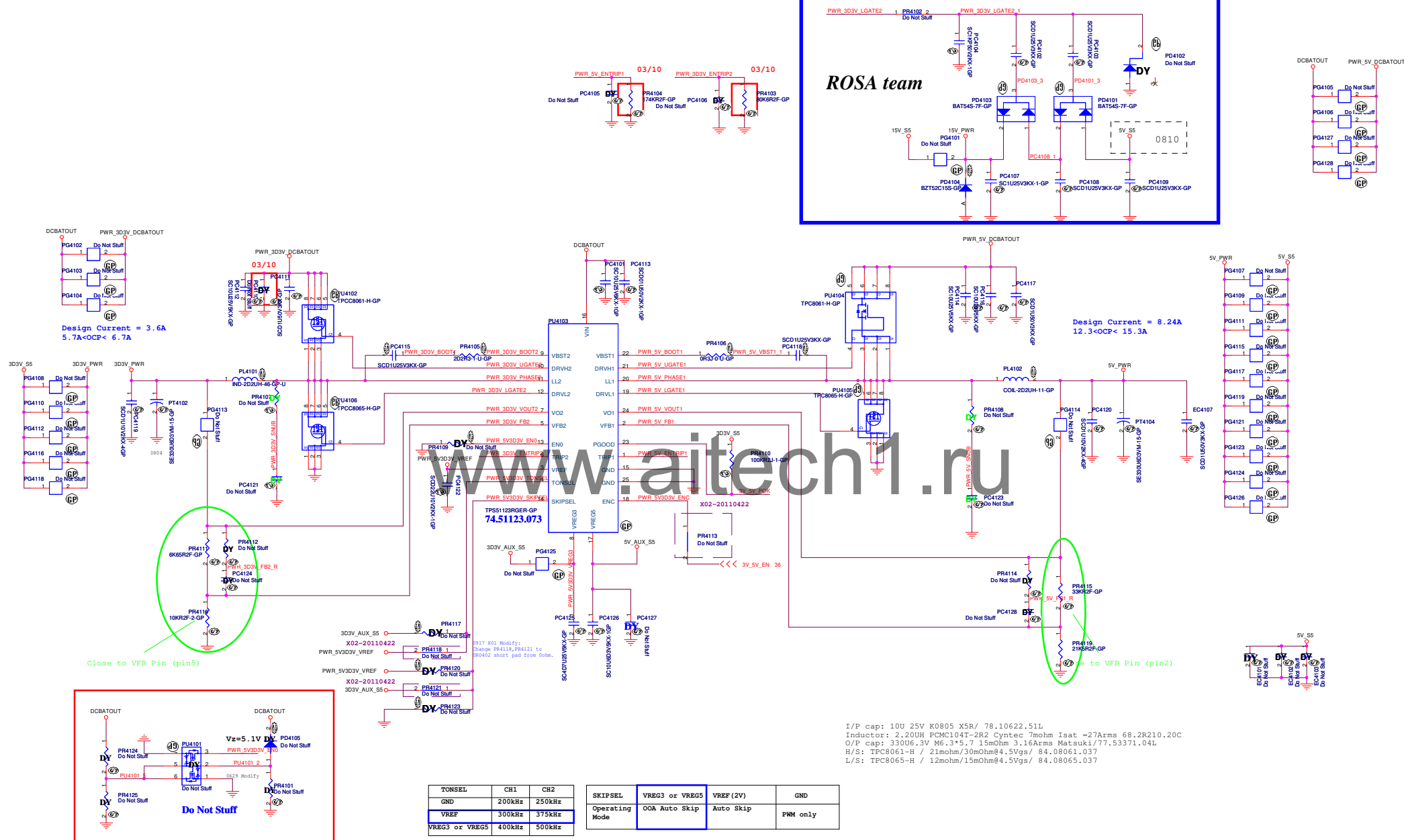
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24707**

Size: Custom Document Number: **Enrico/Caruso 15 HR** Rev: X01

Date: Thursday, June 02, 2011 Sheet: 40 of 104

```
SSID = PWR.Plane.Regulator_5v3p3v
```




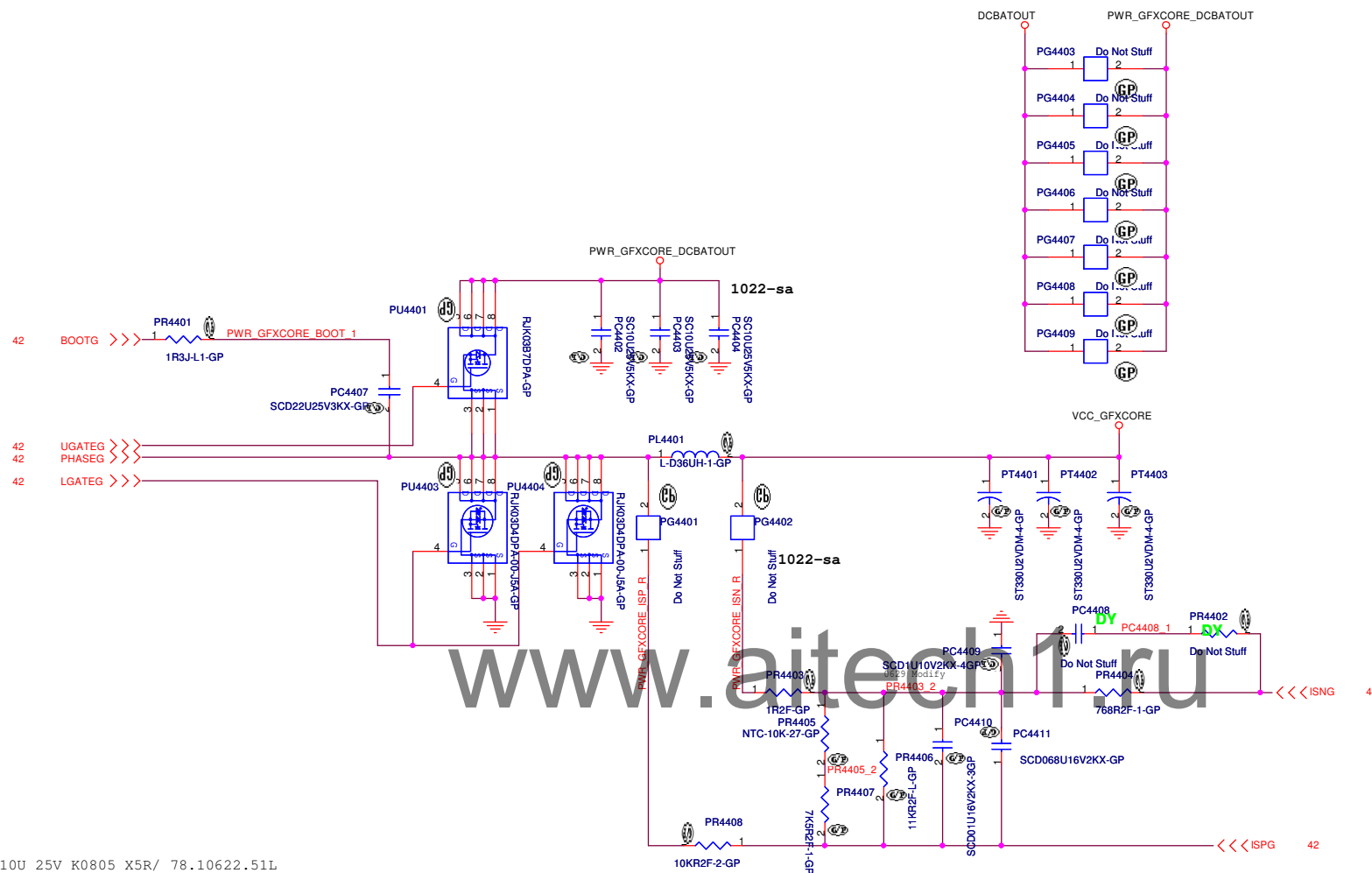
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PFCM0637-2R22M Cyntec 20mohm Isat =14Arms 68.2R210.20B
O/P cap: 3300u.3V M6.3*5.7 15mohm 3.16Arms Matsuki/77.53371.04L
H/S: TPC8061-H NC 8P / 21mohm/29mohm@4.5Vgs/ 84.08061.A37
L/S: TPC8065-H NC 8P / 12.1mohm/17.4mohm@4.5Vgs/ 84.08065.A37

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPC8061-H / 21mohm/30mOhm@4.5Vgs/ 84.08061.037
L/S: TPC8065-H / 12mohm/15mOhm@4.5Vgs/ 84.08065.037

DV15 HR Vos GIGA HDMI NoSurp



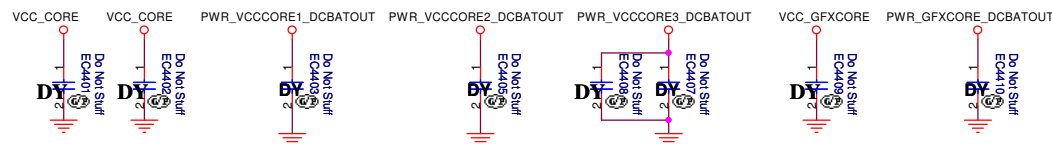
 <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div>			
Title ISL95831 CPU CORE(1/3)			
Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
Date: Thursday, June 02, 2011		Sheet 42 of	104



VCC_GFXCORE
I_{omax}=33A
OCP>50A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: RJK03B7DPA NC WPAK 8P/7.7mOhm/10.7mOhm@4.5Vgs/84.003B7.037
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

EMI/ESD



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ISL95831 CPU CORE(3/3)

Size
A3

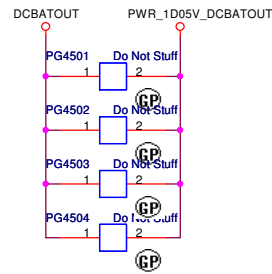
Document Number

Enrico/Caruso 15 HR

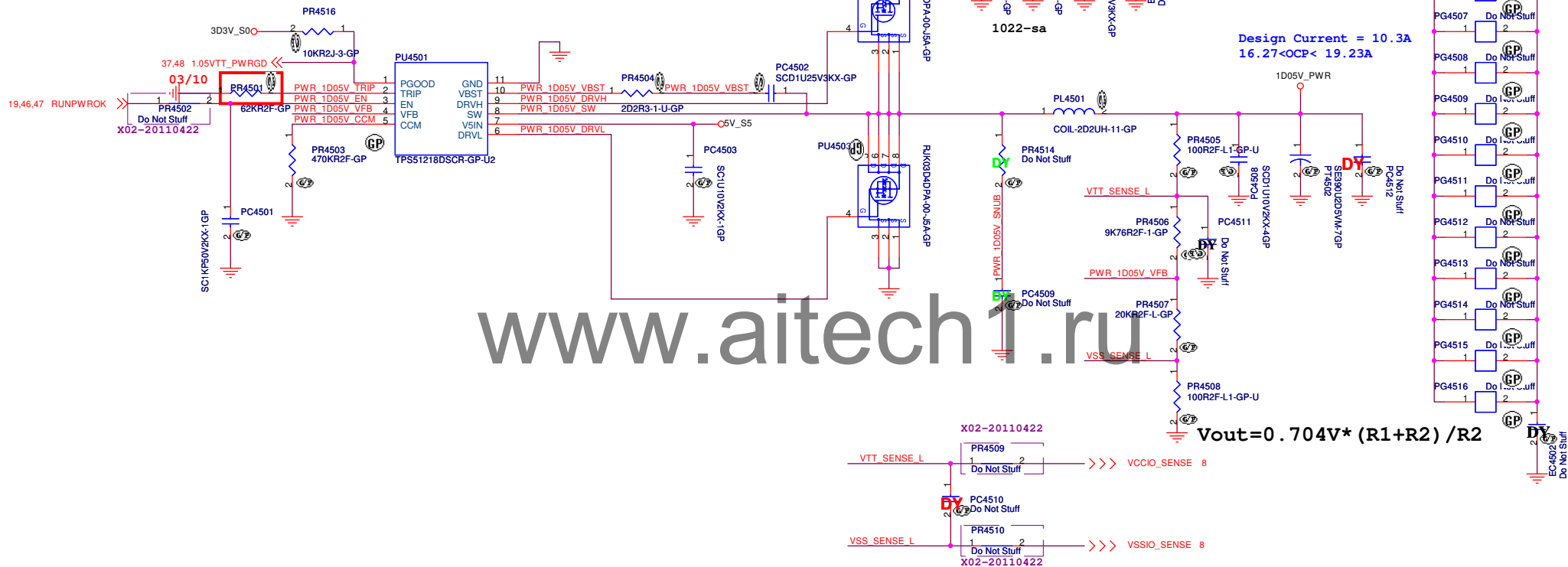
Rev
X01

Date: Thursday, June 02, 2011

Sheet 44 of 104



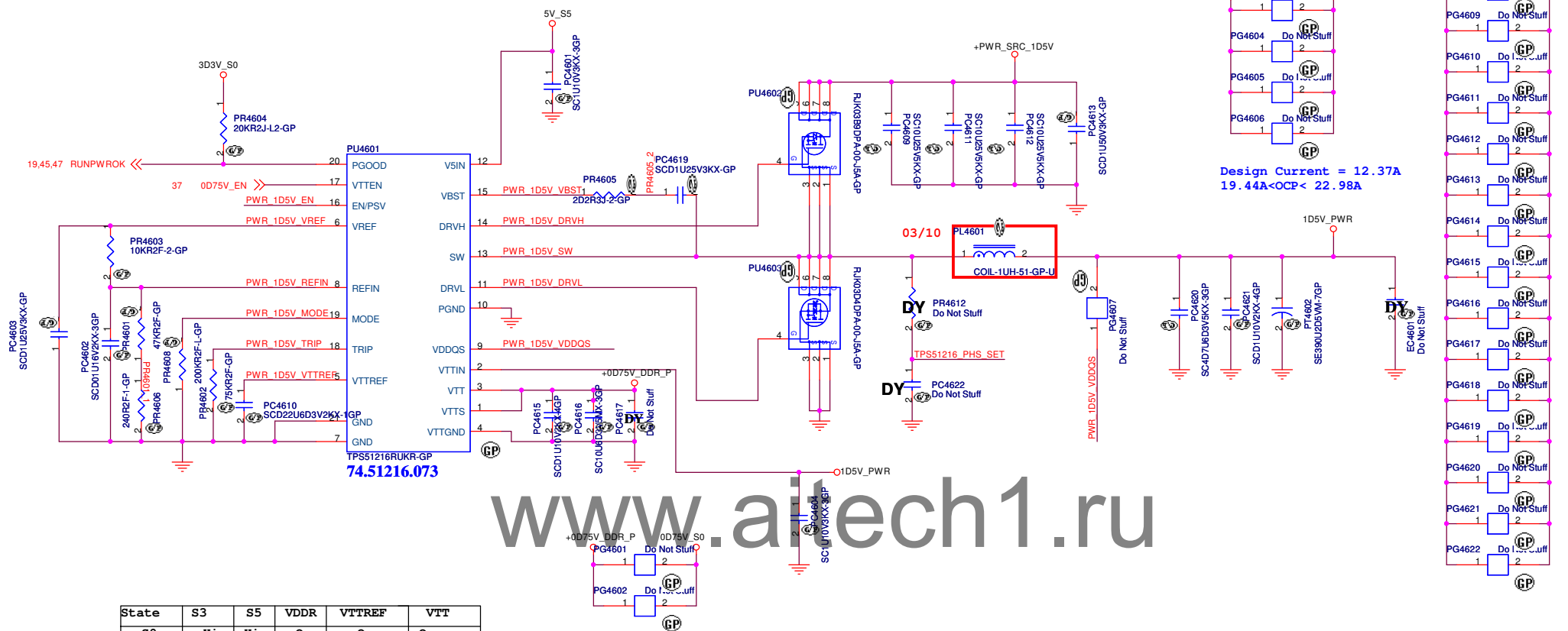
TPS51218 for 1D05V



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.20UH PCMC104T-2R2 Cyntec 7mohm Isat =27Arms 68.2R210.20C
 O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

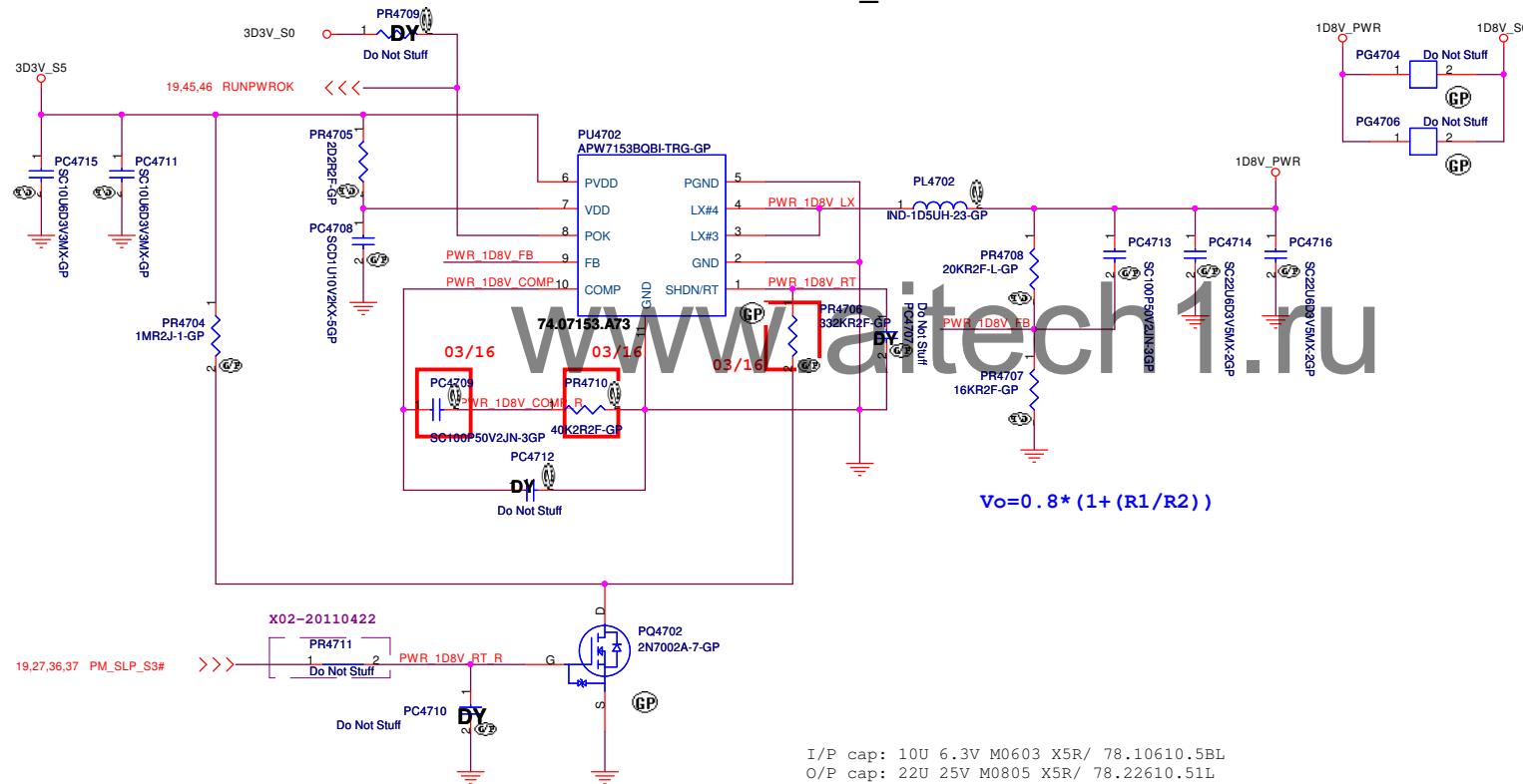
MODE		
PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.0UH PCMB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/ 79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/ 10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RUK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

SSID = PWR.Plane.Regulator_1D8V_S0

+1.8V_RUN
Design current = 0.87A

APW7153B for 1D8V_S0



I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

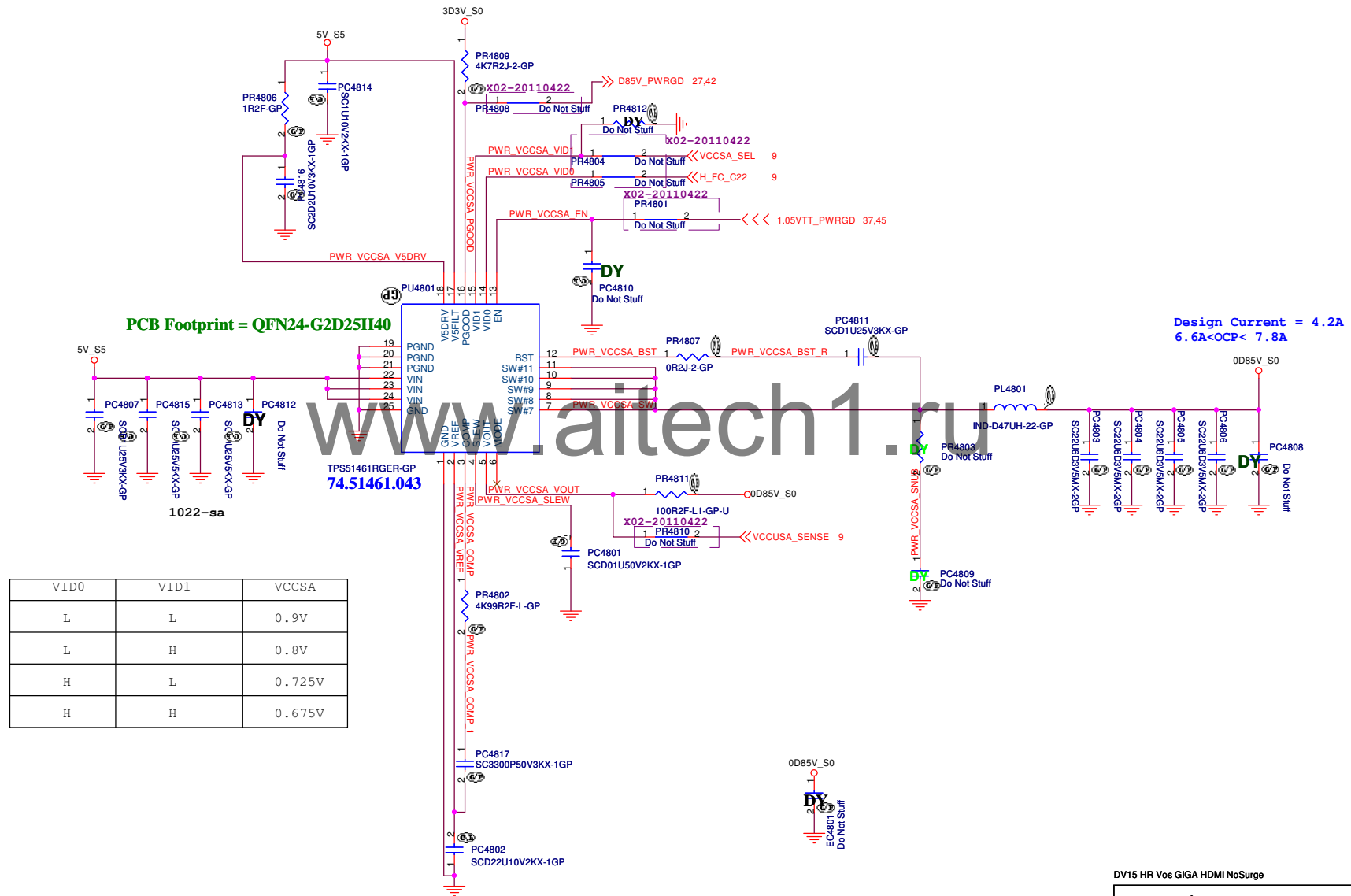
DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

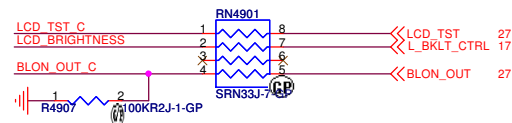
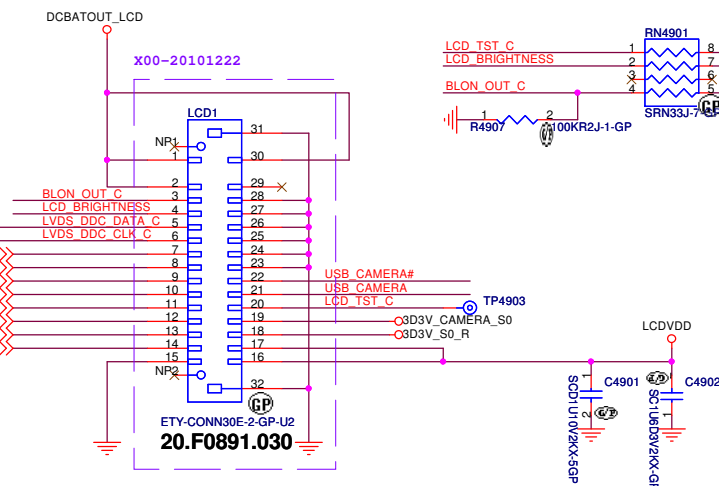
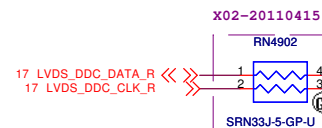
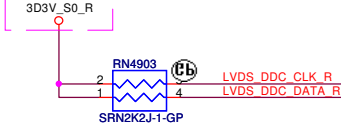
Title			TPS51311 for 1D8V_S0	
Size	Document Number	Rev		
A3		Enrico/Caruso 15 HR		X01
Date:	Thursday, June 02, 2011	Sheet	47	of 104

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

X01-20110307



DCBATOUT

F4901 POLYSW-1D1A24V-GP-U

DCBATOUT_LCD

69.50007.A31
2nd = 69.50007.A41

C4905 SCD1U50V3KX-GP

C4904 SC1KP50V2KX-1GP

3D3V_S0

3D3V_CAMERA_S

X01-20110302

R4933

1

0R3J-0-U-GP

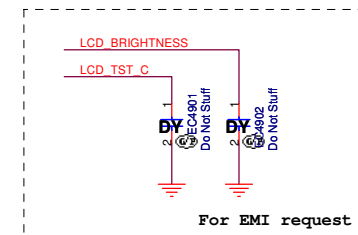
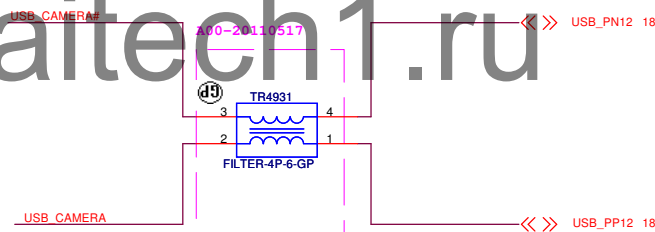
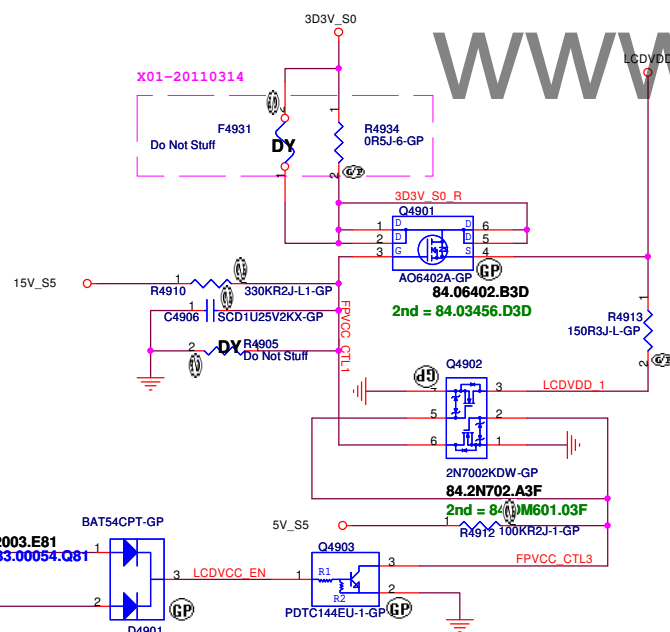
C4903

SC10U6D3V5MX-3GP

EC4903

BY

Do Not Stuff

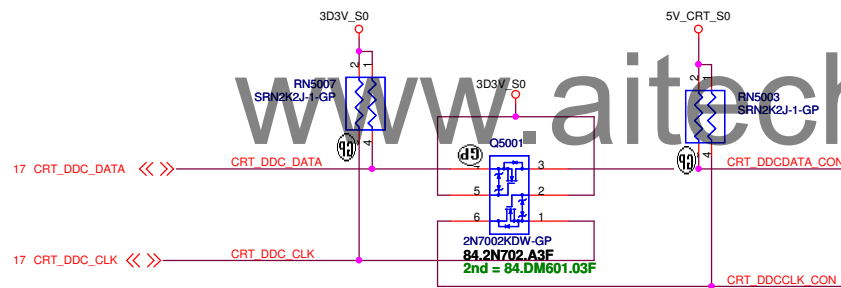
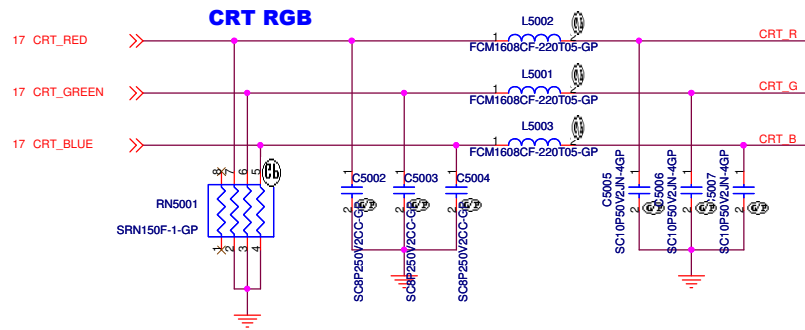


SSID = VIDEO

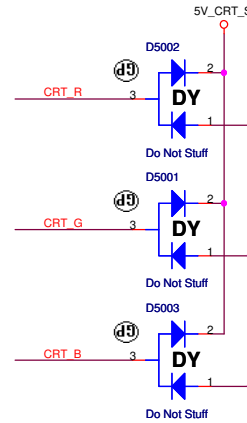
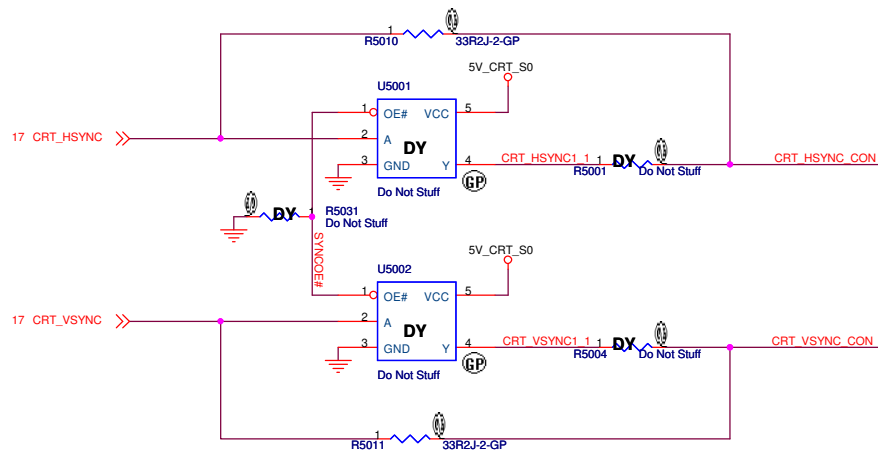
Layout Note:

*Pi-filter & 150 Ohm pull-down
resistors should be as close
as to CRT CONN.

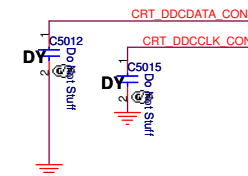
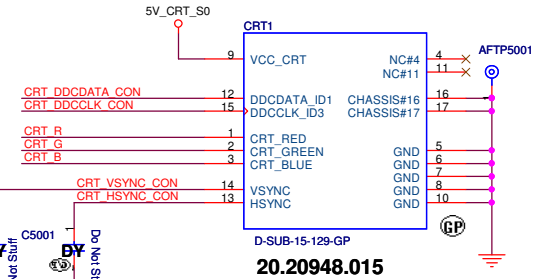
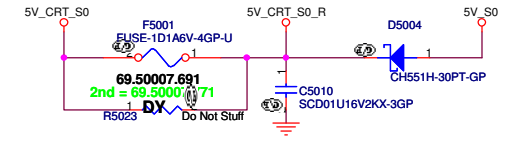
* RGB signal will hit 75 Ohm
first, then pi-filter, finally
CRT CONN.



Hsync & Vsync



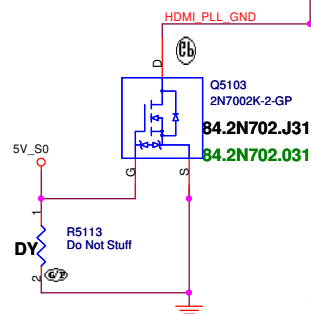
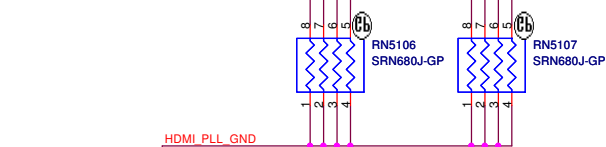
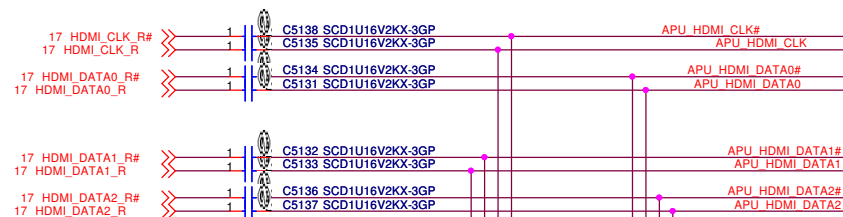
AFTP5002 1 5V_CRT_S0
AFTP5003 1 CRT_DDCDATA_CON
AFTP5004 1 CRT_DDCCLK_CON
AFTP5005 1 CRT_R
AFTP5006 1 CRT_G
AFTP5007 1 CRT_B
AFTP5008 1 CRT_HSYNC_CON
AFTP5009 1 CRT_VSYNC_CON



DV15 HR Vos GIGA HDMI NoSurge

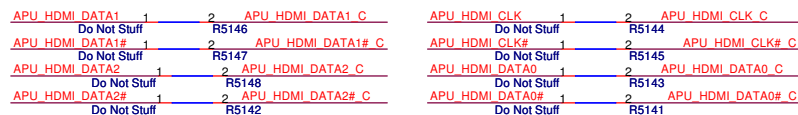
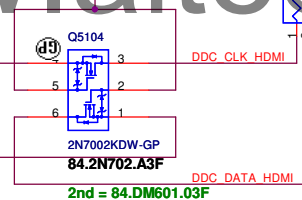
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title CRT Connector			
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 HR	X01	
Date: Thursday, June 02, 2011	Sheet 50	of 104	

SSID = VIDEO



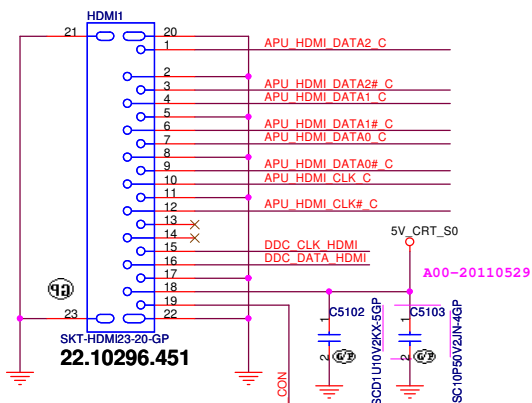
17 PCH_HDMI_CLK >>

17 PCH_HDMI_DATA <<>



A00-20110530

HDMI CONN



5V_CRT_S0



Do Not Stuff

R5110

DY

84.03904.L06

2nd = 84.03904.P11

3rd = 84.03904.T11

HDMI_HPD_B

150KR2JL1-GP

R5111

HDMI_HPD_E

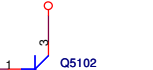
1

2

Do Not Stuff

HDMI_PCH_DET 17

3D3V_S0



DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shifter/Connector**

Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet 51 of 104

www.aitech1.ru



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Reserved

Document Number **Enrico/Caruso 15 HB**

Rev
X01

Sheet 52 of 104

(Blanking)

www.aitech1.ru


www.aitech1.ru

SSID = User.Interface

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP/Fan Connector

Size
A3

Document Number
Enrico/Caruso 15 HR

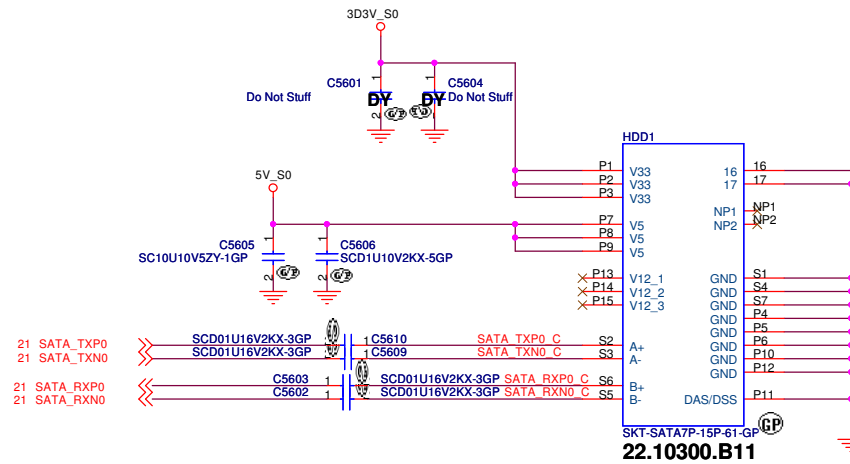
Date: Thursday, June 02, 2011

Rev
X01

Sheet 55 of 104

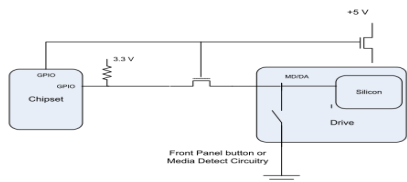
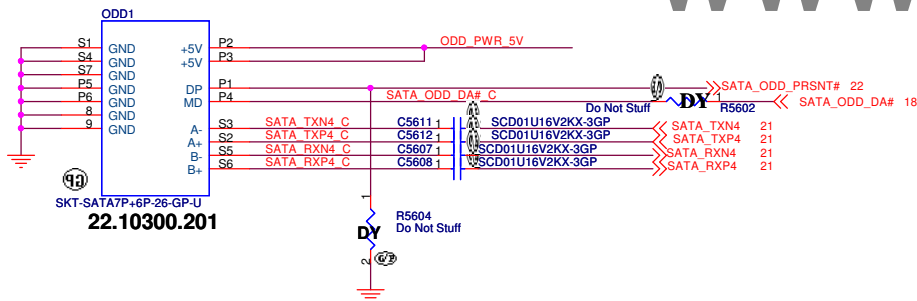
SSID = SATA

SATA HDD Connector



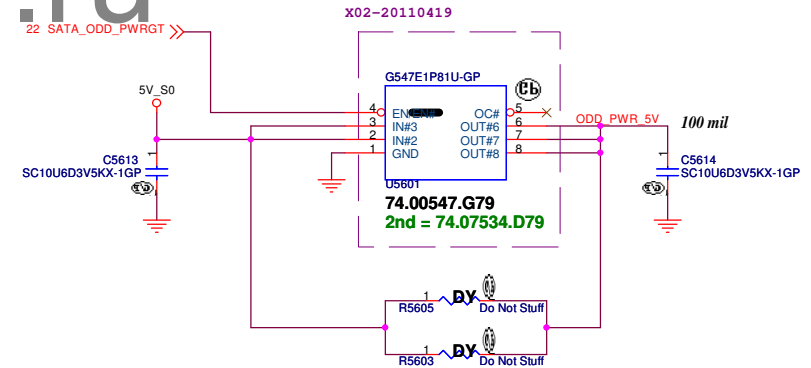
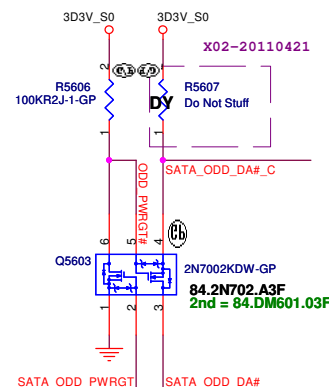
ODD Connector

www.aitech1.ru



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SUPPORT ZERO SATA ODD



DV15 HR Vos GIGA HDMI NoSurge


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD/ODD			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 HR	X01	
Date:	Thursday, June 02, 2011	Sheet	56 of 104

SSID = ESATA

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ESATA

Size
A3

Document Number

Date: Thursday, June 02, 2011

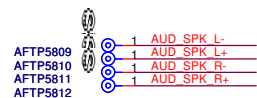
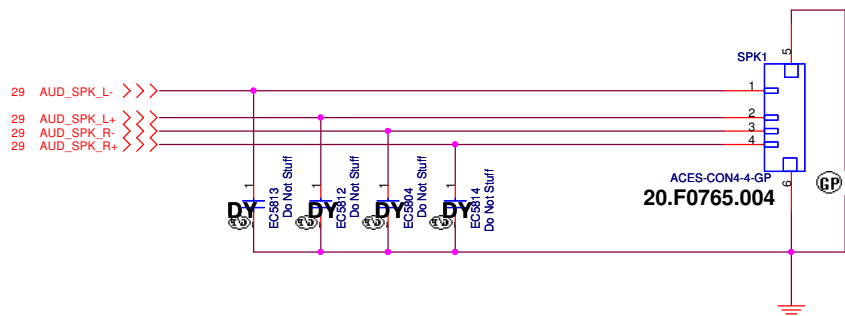
Enrico/Caruso 15 HR

Sheet 57 of 104

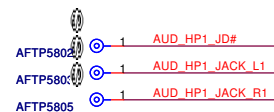
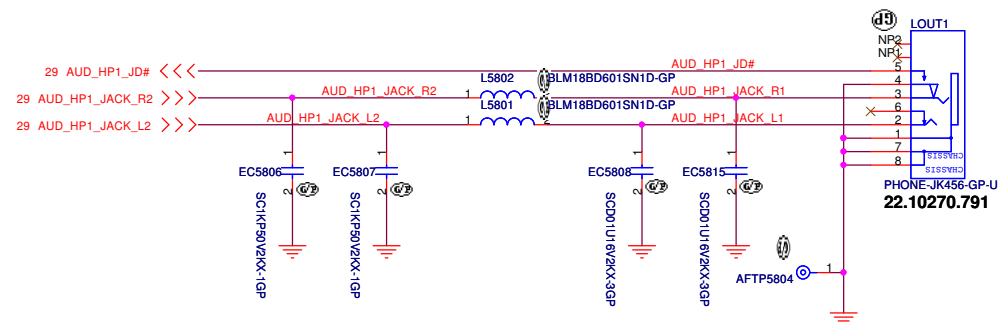
Rev
X01

SSID = AUDIO

Speaker Connector



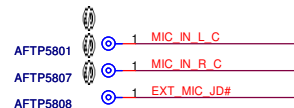
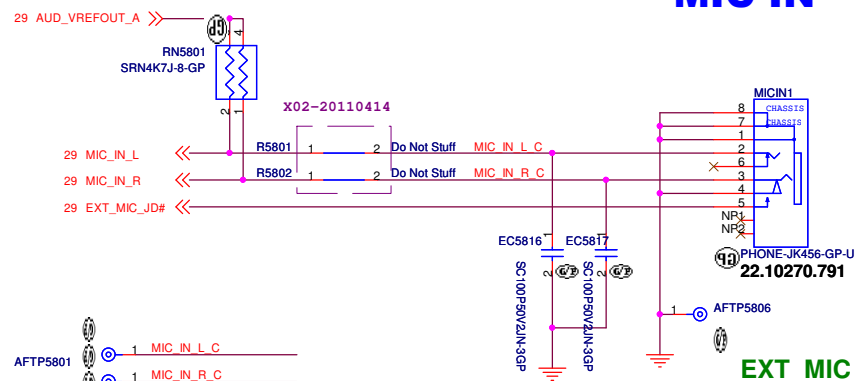
LINE1 OUT



AUD_HP1_JD#
Normal Open

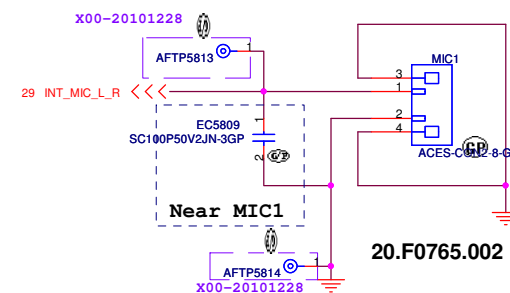
www.aitech1.ru

MIC IN



EXT_MIC_JD#
Normal Open

Internal Microphone



20.F0765.002

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SPEAKER CONN

Size

Document Number

Enrico/Caruso 15 HR

Rev

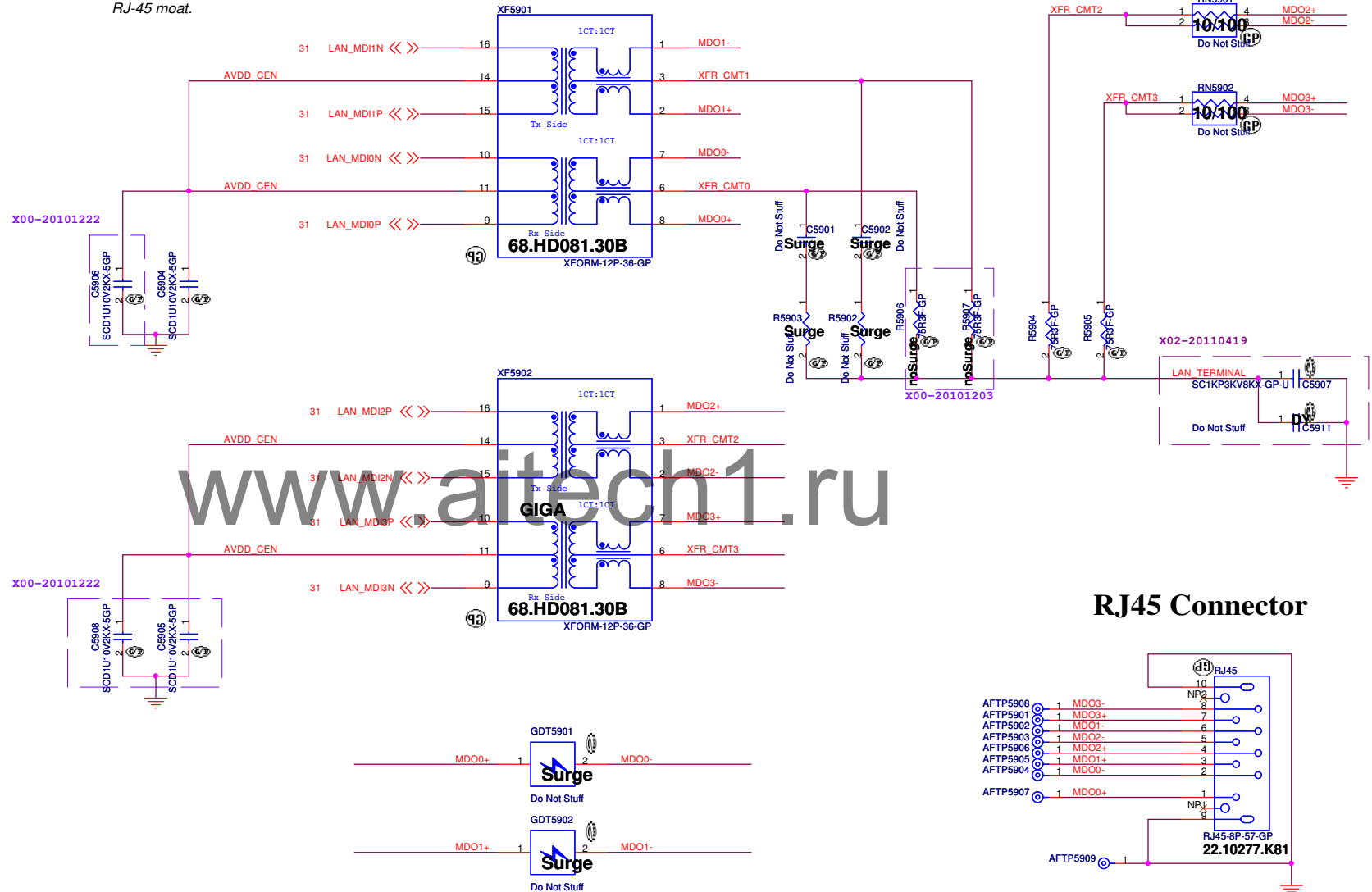
X01

Date: Thursday, June 02, 2011

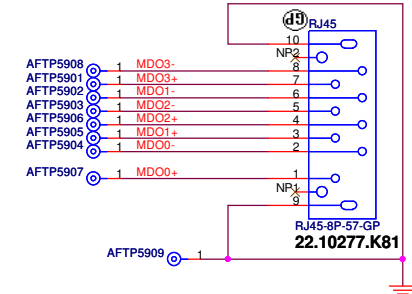
Sheet 58 of 104

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer



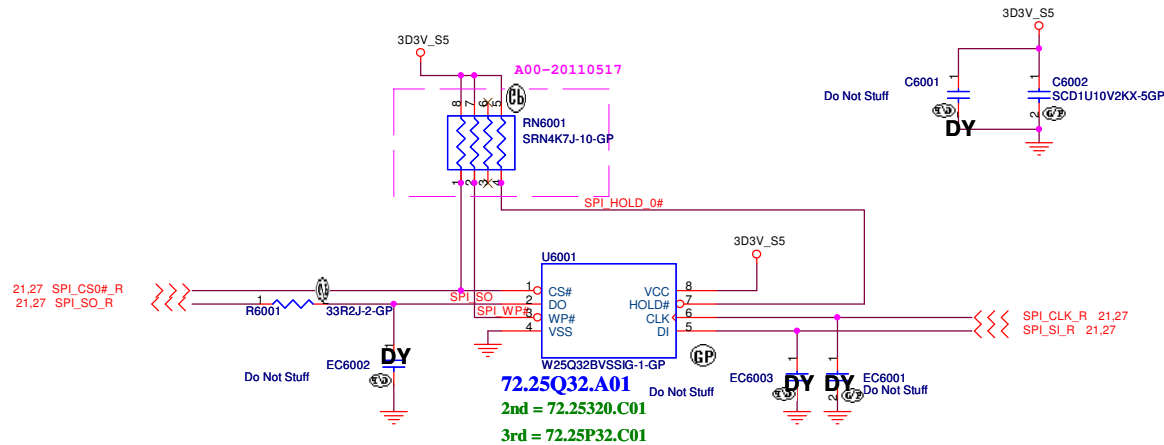
RJ45 Connector



DV15 HR Vos GIGA HDMI NoSurge

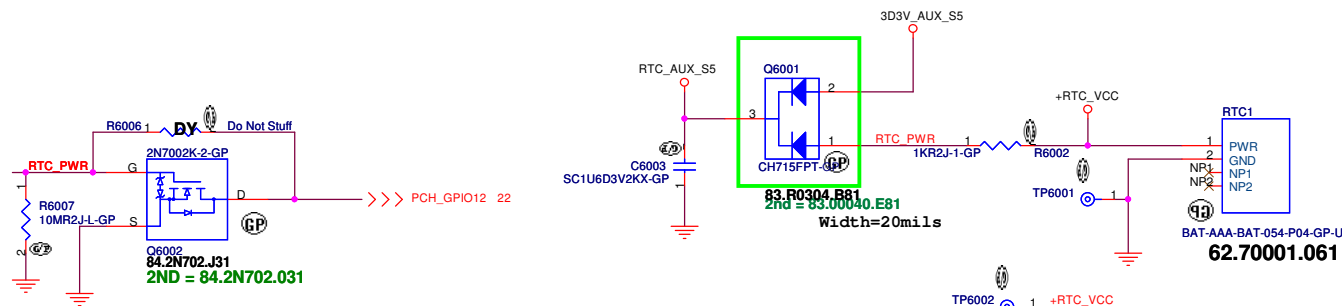
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



www.aitech1.ru

SSID = RBATT



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size	A3
------	----

Document Number

Enrico/Caruso 15 HR

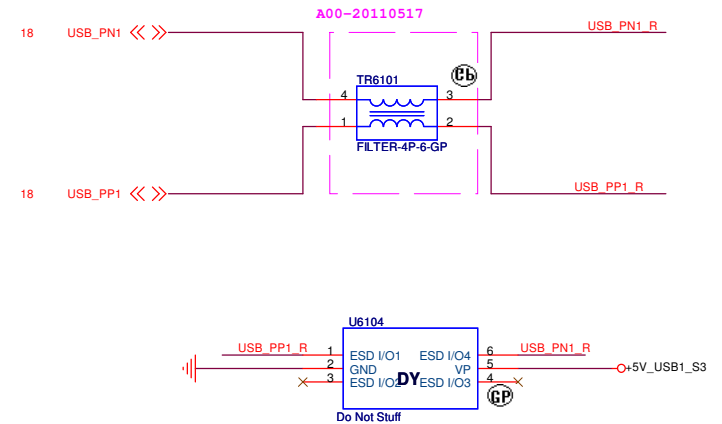
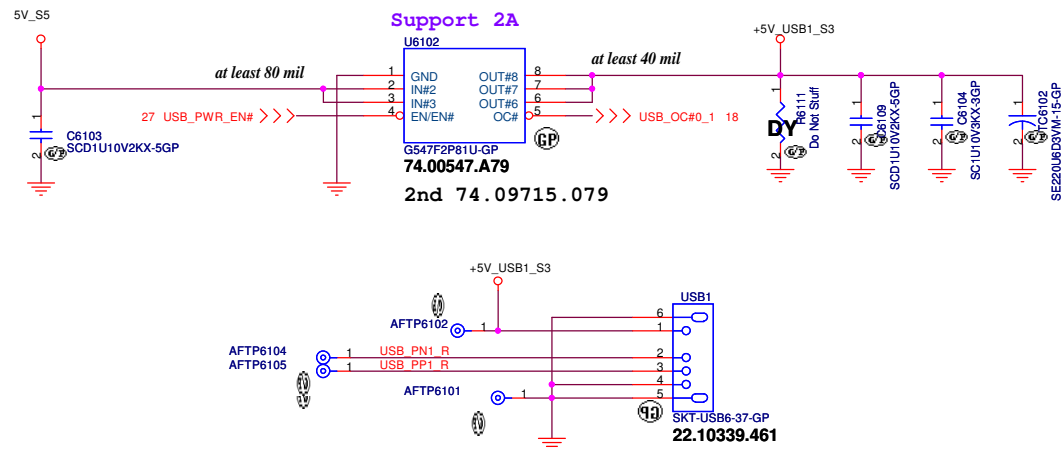
Rev	X01
-----	-----

Date: Thursday, June 02, 2011

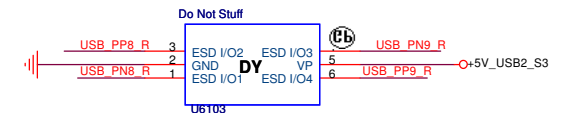
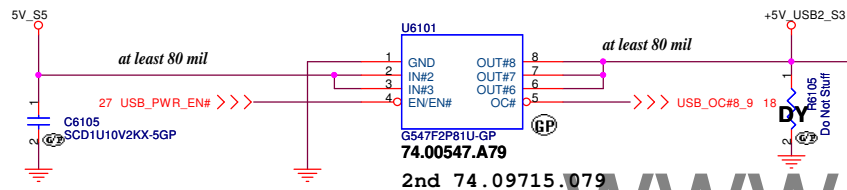
Sheet	60	of	104
-------	----	----	-----

SSID = USB

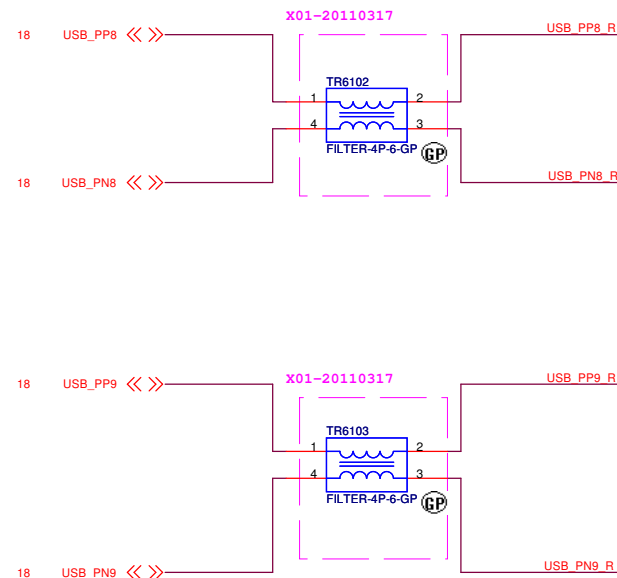
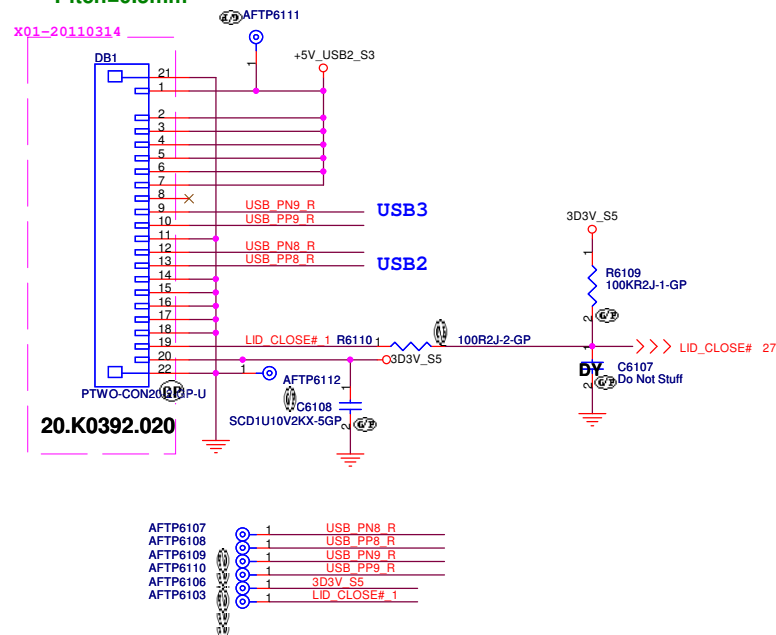
Left USB Power x1



Right USB Power x2



Pitch=0.5mm



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB Power SW			
Size	Document Number		Rev
	Enrico/Caruso 15 HR		X01
Date: Thursday, June 02, 2011	Sheet	61 of	104

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved


Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01

Date: Thursday, June 02, 2011	Sheet 62 of 104
-------------------------------	-----------------

SSID = User.Interface

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Bluetooth			
Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
Date: Thursday, June 02, 2011		Sheet 63	of 104

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge

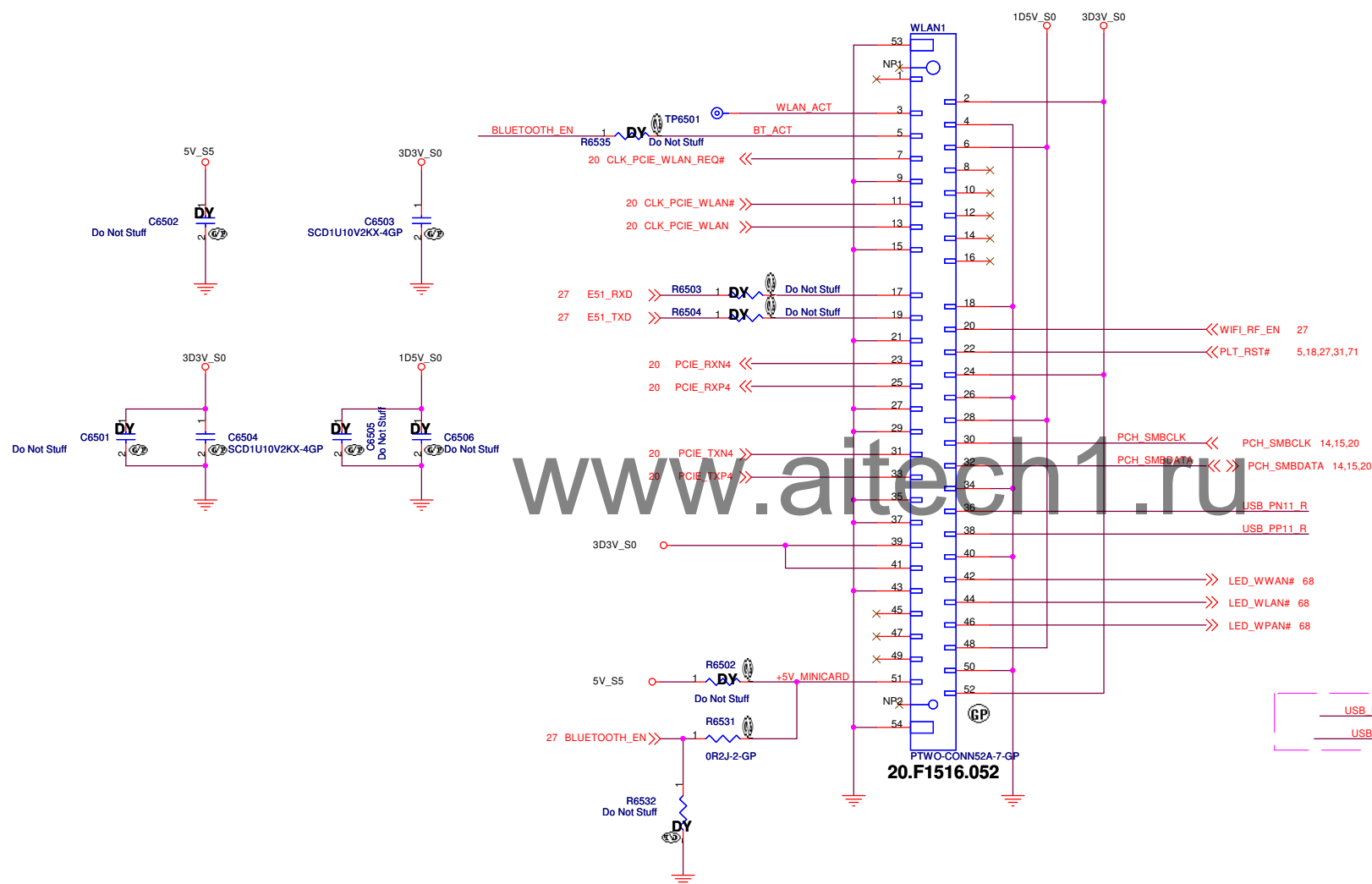


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			RESERVED	
Size	Document Number	Rev		
A3	Enrico/Caruso 15 HR	X01		
Date:	Thursday, June 02, 2011	Sheet	64	of 104

SSID = Wireless

Mini Card Connector(802.11b/g/n)



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A3

Document Number

Enrico/Caruso 15 HR

Rev

X01

Date: Thursday, June 02, 2011

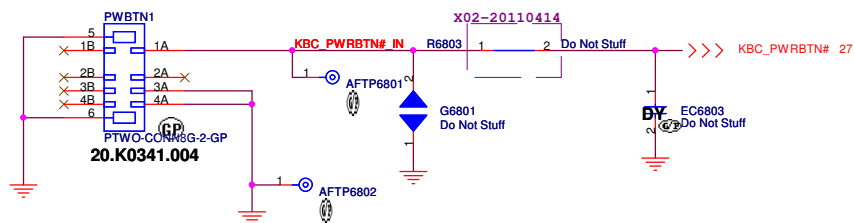
Sheet 65 of 104

www.aitech1.ru

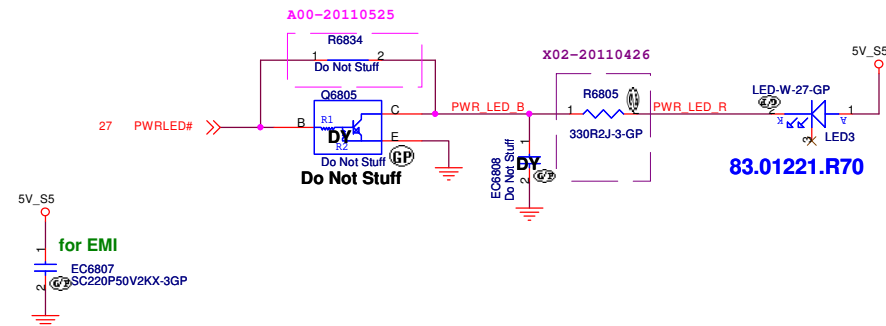
(Blanking)

www.aitech1.ru

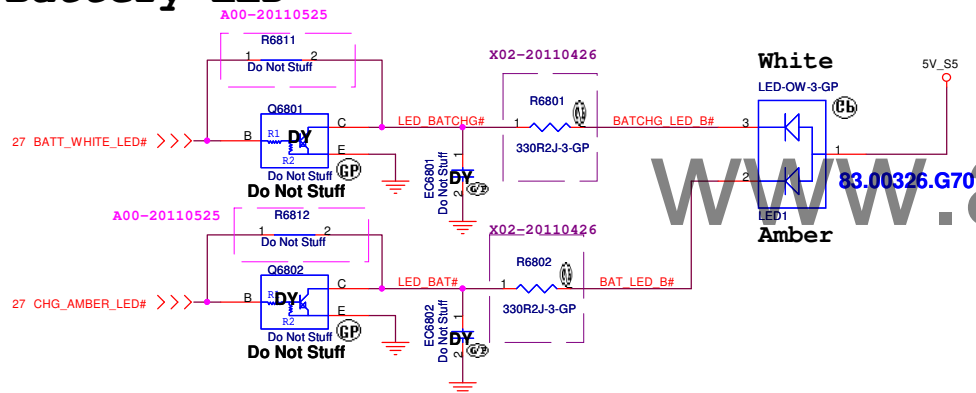
Power BTN Connector



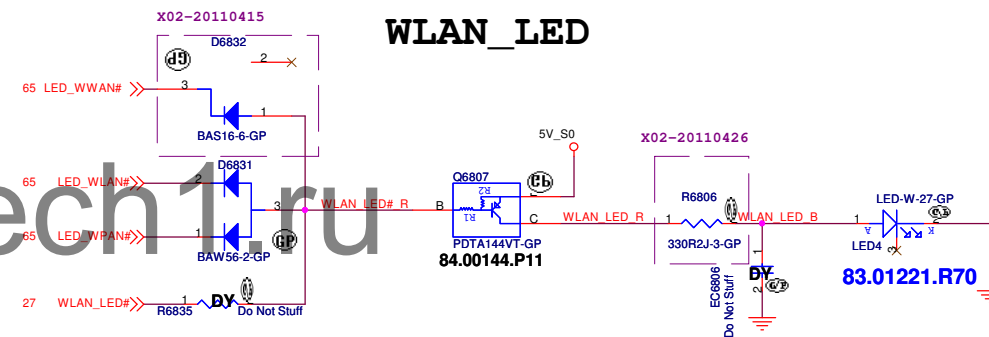
Power LED



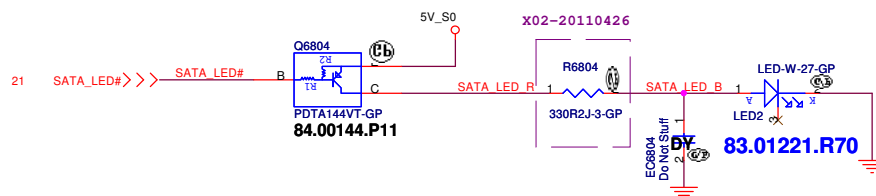
Battery LED



WLAN LED



HDD LED



LED Location from left to right
(MB, Top View)

LED3 LED2 LED1 LED4
PWR HDD Battery WiFi

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LED Bard/Power Button

Size
A3

Document Number

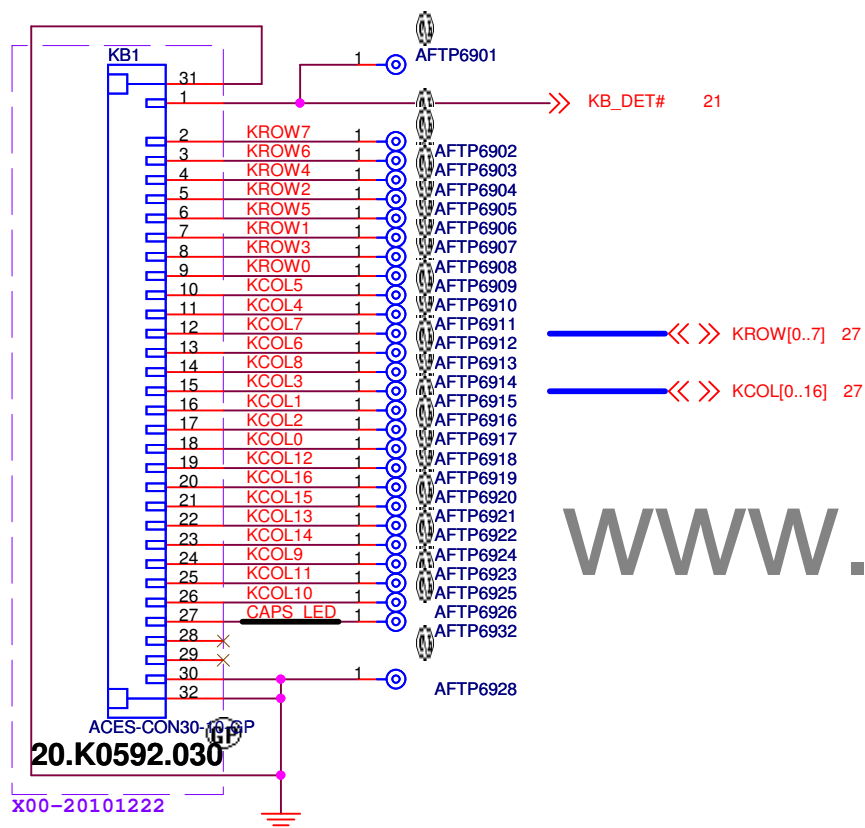
Enrico/Caruso 15 HR

Rev
Y01

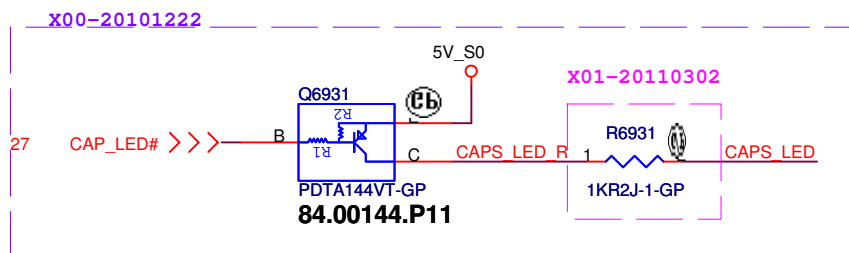
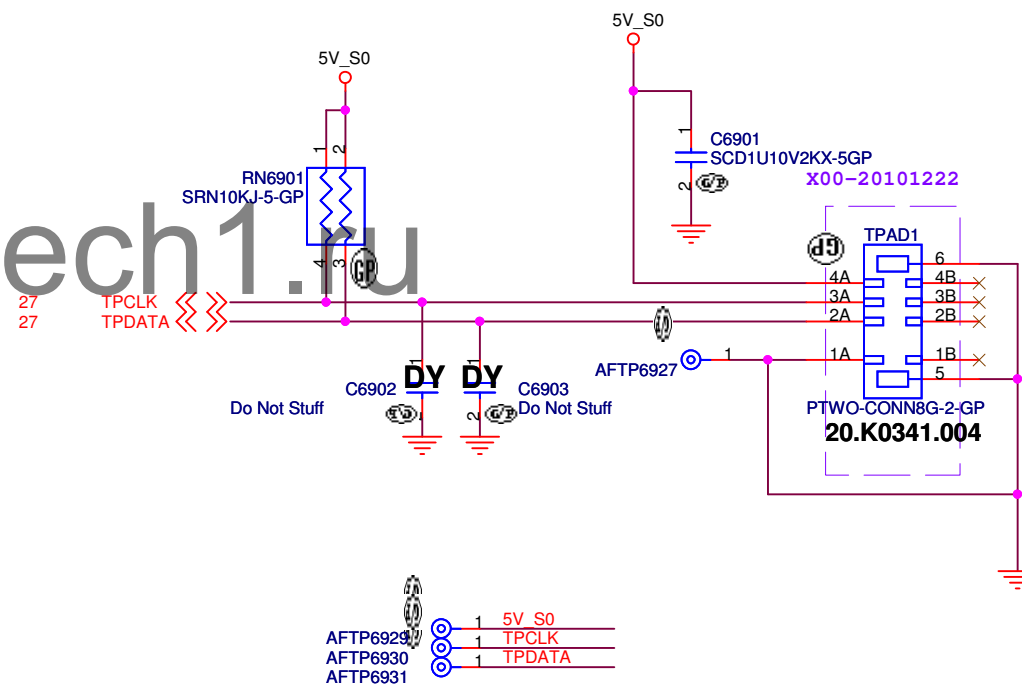
Date: Thursday, June 02, 2011

Sheet 68 of 104

Internal KeyBoard Connector



TouchPad Connector



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size

Document Number

Rev

Enrico/Caruso 15 HR

X01

Date: Thursday, June 02, 2011

Sheet 69 of 104

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A3

Document Number

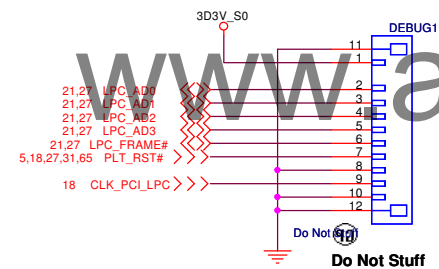
Enrico/Caruso 15 HR

Rev

X01

Date: Thursday, June 02, 2011

Sheet 70 of 104



DV15 HR Vos GIGA HDMI NoSurge

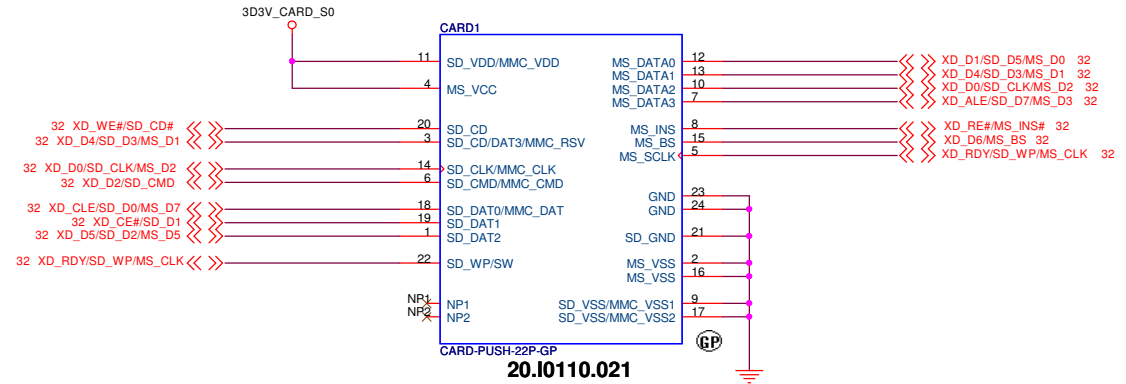
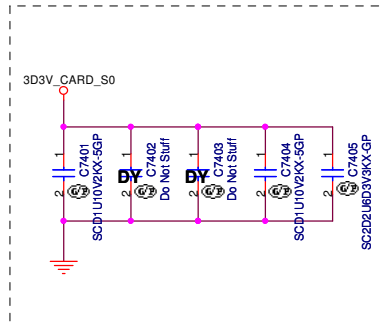
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Dubug connector			
Size A3	Document Number		Rev X01
Date: Thursday, June 02, 2011			
Sheet 71		of 104	

www.aitech1.ru

www.aitech1.ru

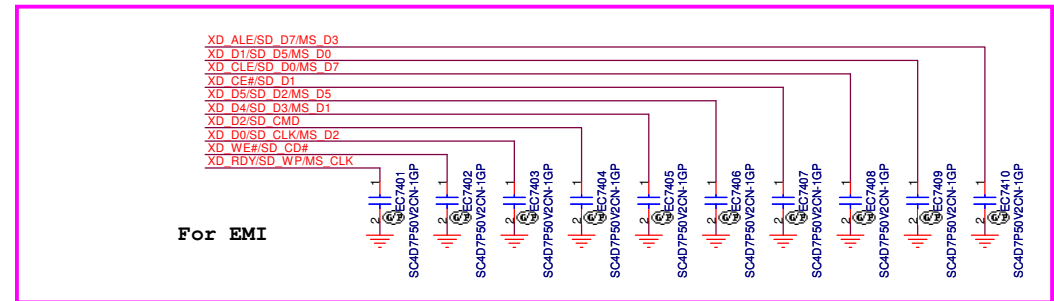
SSID = SDIO

SD/MMC/MS Card Reader



www.aitech1.ru

X01-20110315



DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			SD/MS/MMC Card CONN
Size	Document Number	Rev	X01
A3	Enrico/Caruso 15 HR		
Date:	Thursday, June 02, 2011	Sheet	74 of 104

SSID = ExpressCard

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Express Card			
Size A3	Document Number		Rev X01
Date: Thursday, June 02, 2011		Sheet 75 of	104

www.aitech1.ru

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Enrico/Caruso 15 HR

Rev
X01

Date: Thursday, June 02, 2011Sheet 77 of 104

www.aitech1.ru

SSID = User.Interface

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Free Fall Sensor	
Size	Document Number			Rev
A3	Enrico/Caruso 15 HR		X01	
Date: Thursday, June 02, 2011		Sheet	79	of 104

www.aitech1.ru



Reserved

Doc A3	Document Number	Enrico/Caruso 15 HR	Fig. X01
-----------	-----------------	----------------------------	-------------

Sheet	80	of	104
-------	----	----	-----

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Enrico/Caruso 15 HR

Date: Thursday, June 02, 2011


Rev
X01

Sheet 81 of 104

Reserved

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO Board Connector


Size	Document Number	Rev
A3	<i>Enrico/Caruso 15 HR</i>	X01

Date: Thursday, June 02, 2011	Sheet 82 of 104
-------------------------------	-----------------

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU PCIE/STRAPPING(1/5)

Size
A3

Document Number
Enrico/Caruso 15 HR

Date: Thursday, June 02, 2011

Rev
X01

Sheet 83 of 104

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU Memory(2/5)

Size
Custom

Document Number

Enrico/Caruso 15 HR

Rev
X01

Date: Thursday, June 02, 2011

Sheet 84 of 104

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge

DELL		Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File GPU_DP/LVDS/CRT/GPIO(3/5)			
Size K	Document Number Enrico/Caruso 15 HR	Rev X01	
Date: 10/25/09, June 12, 2011	Sheet 82	of 104	

(Blanking)

www.aitech1.ru

(Blanking)

www.aitech1.ru

(Blanking)

www.aitech1.ru


(Blanking)

www.aitech1.ru

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

Size
A3

Document Number
Enrico/Caruso 15 HR

Rev
X01

Date: Thursday, June 02, 2011

Sheet 90 of 104

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM7,8 (4/4)

Size
A3

Document Number

Rev

Enrico/Caruso 15 HR

X01

Date: Thursday, June 02, 2011

Sheet 91 of 104

(Blanking)

www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RT8208B +VGA CORE

Size

A3

Document Number

Enrico/Caruso 15 HR

Rev

X01

Date: Thursday, June 02, 2011


Sheet 92 of 104

(Blanking)

www.aitech1.ru

(Blanking)
www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Enrico/Caruso 15 HR

Rev
X01

Date: Thursday, June 02, 2011


Sheet 94 of 104

www.aitech1.ru

SSID = SDIO

(Blanking)
www.aitech1.ru

DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

Size
A3

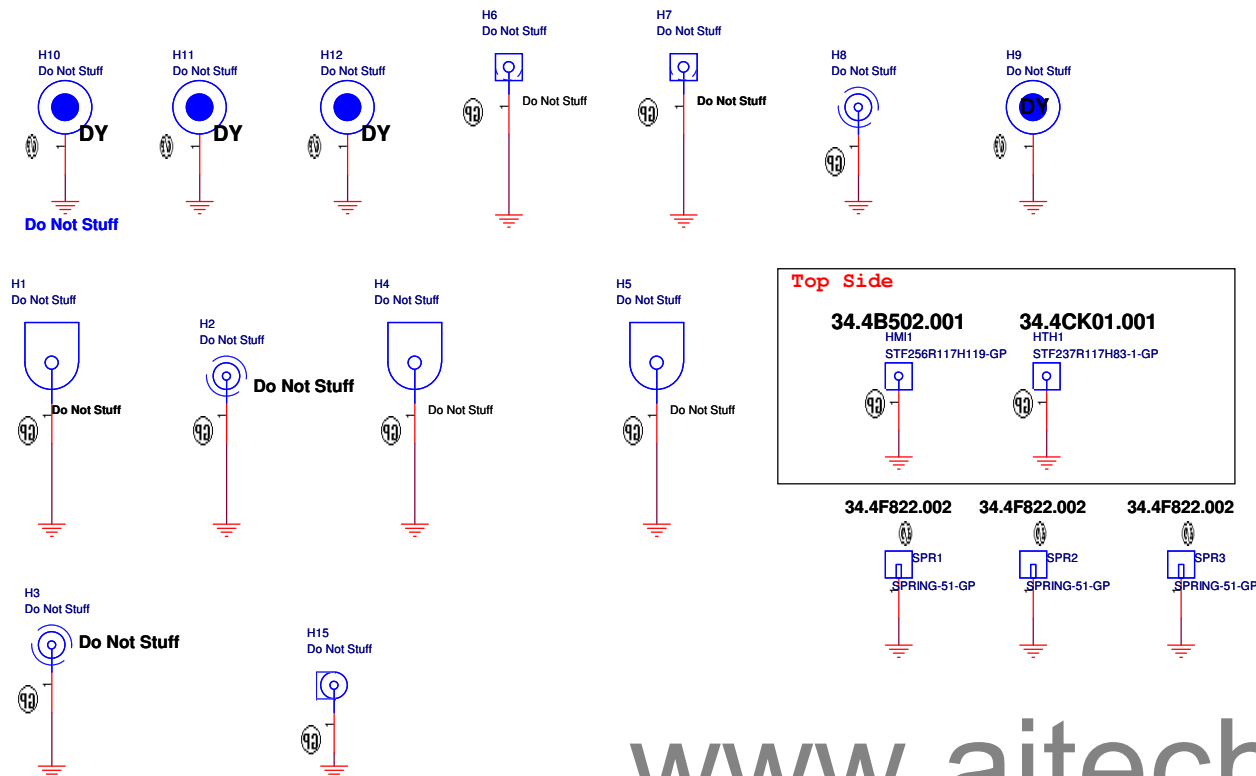
Document Number
Enrico/Caruso 15 HR

Rev
X01

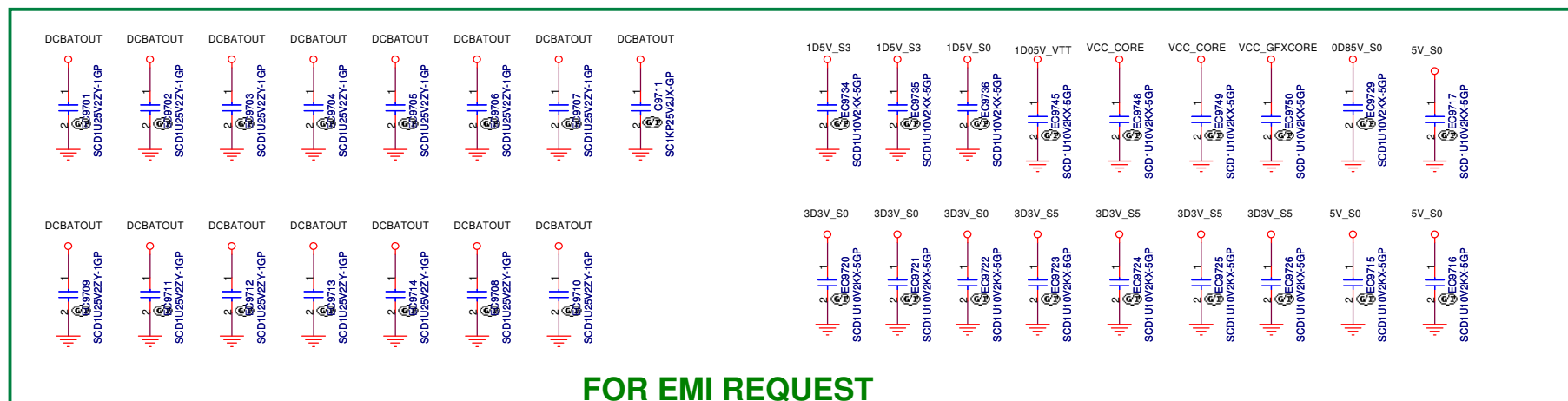
Date: Thursday, June 02, 2011

Sheet 96 of 104

SSID = Mechanical



www.aitech1.ru



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title UNUSED PARTS/EMI Capacitors		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 97 of	104

(AC mode)

Within logic high level and disable if it is less than the logic low level.

Ta

VREF_{bus} must be powered up before VocRef₃, or after VocRef₃ within 0.7 V. Also, VREF_{bus} must power down after VocRef₃, or before VocRef₃ within 0.7 V.

Not floating.

Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.

Tb
V5REF must be powered up before Vcc1_3, or after Vcc1_3 within 0.7 V. Also, V5REF must power down after Vcc1_3, or before Vcc1_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



Sense the power button status

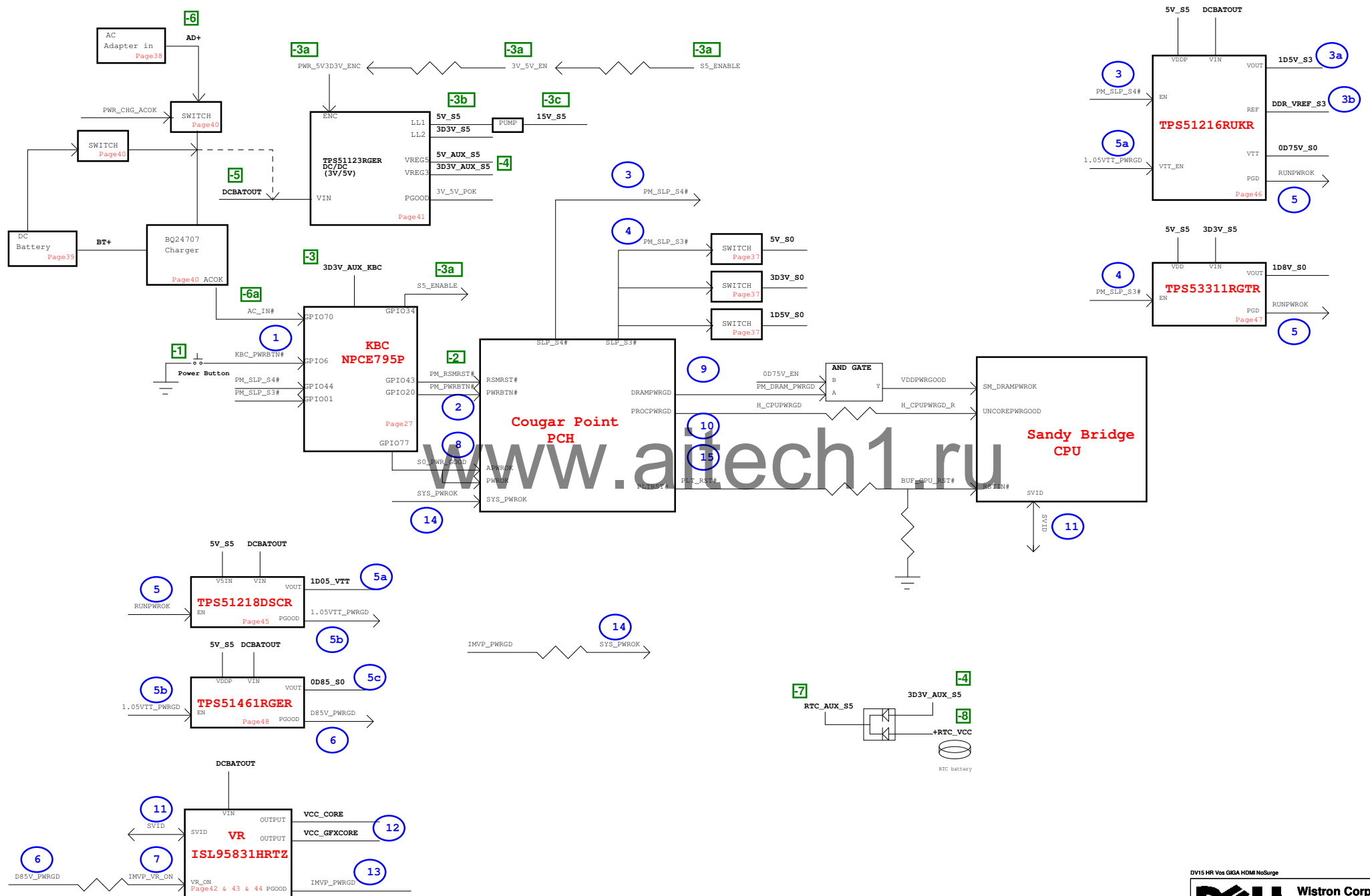
VSRX₃ must be powered up before Voc_{hs1_3}, or after Voc_{hs1_3} within 0.7 V. Also, VSRX₃ must power down after Voc_{hs1_3}, or before Voc_{hs1_3} within 0.7 V.

V18KF must be powered up before Vcc1_3, or after Vcc1_3 within 0.7 V. Also, V18KF must power down after Vcc1_3, or before Vcc1_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-graphics power rails.



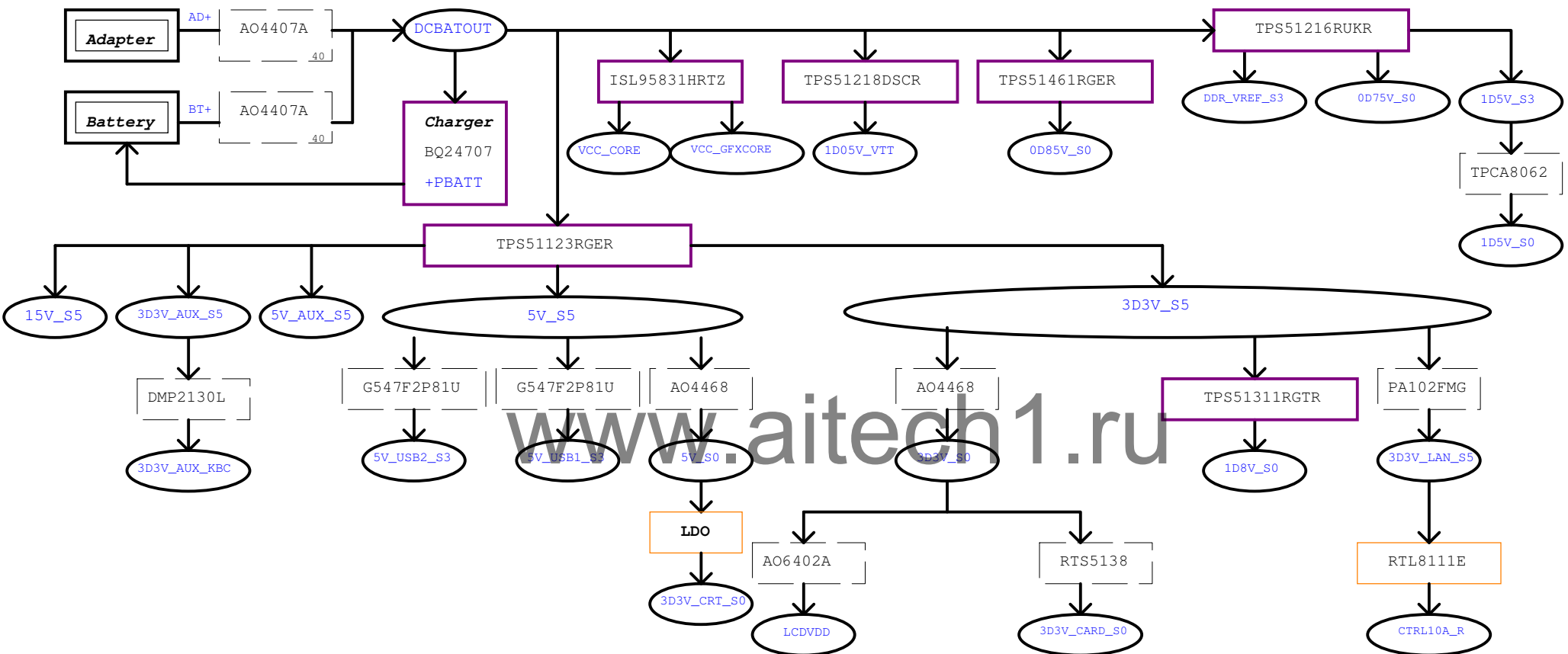
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



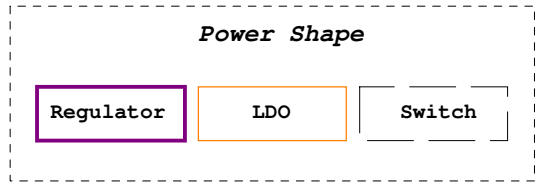
Power Up Sequence: -8 ~ 15

DV15 HR Vos GIGA HDMI NoSurge

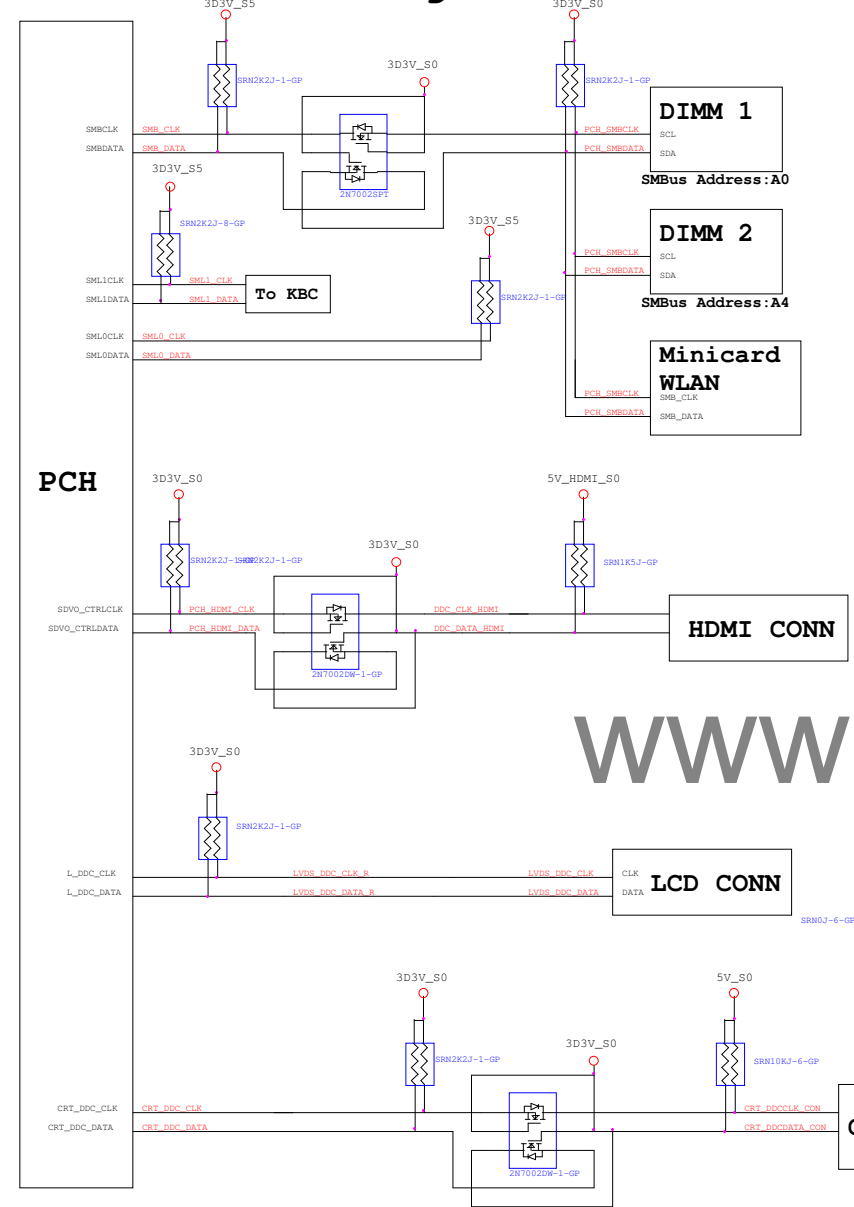
DELL		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power Sequence Diagram			
Size A2	Document Number	Rev	
	Enrico/Caruso 15 HR	X01	
Date: Thursday, June 02, 2011		Sheet	99 of 104



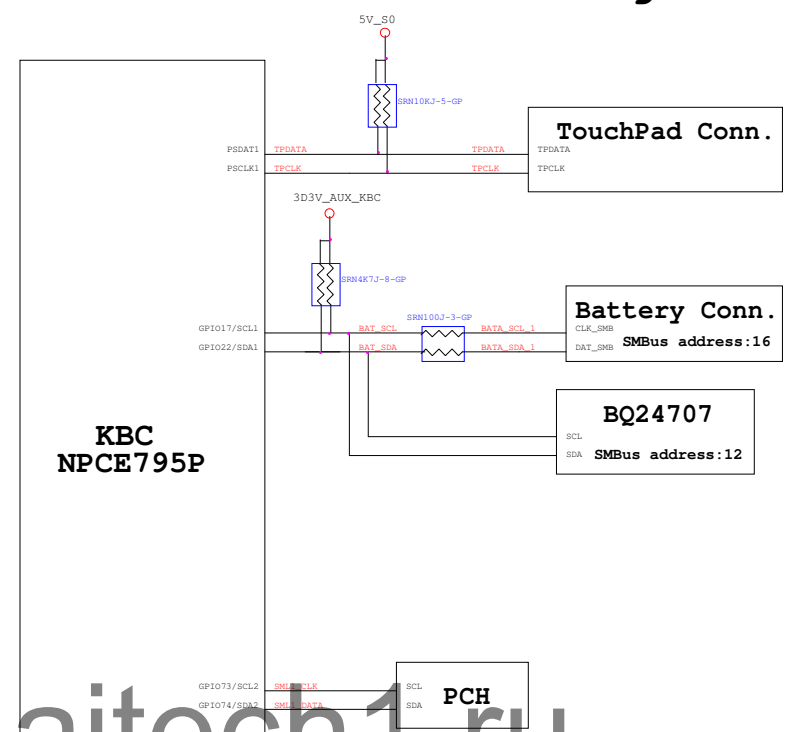
www.aitech1.ru



PCH SMBus Block Diagram

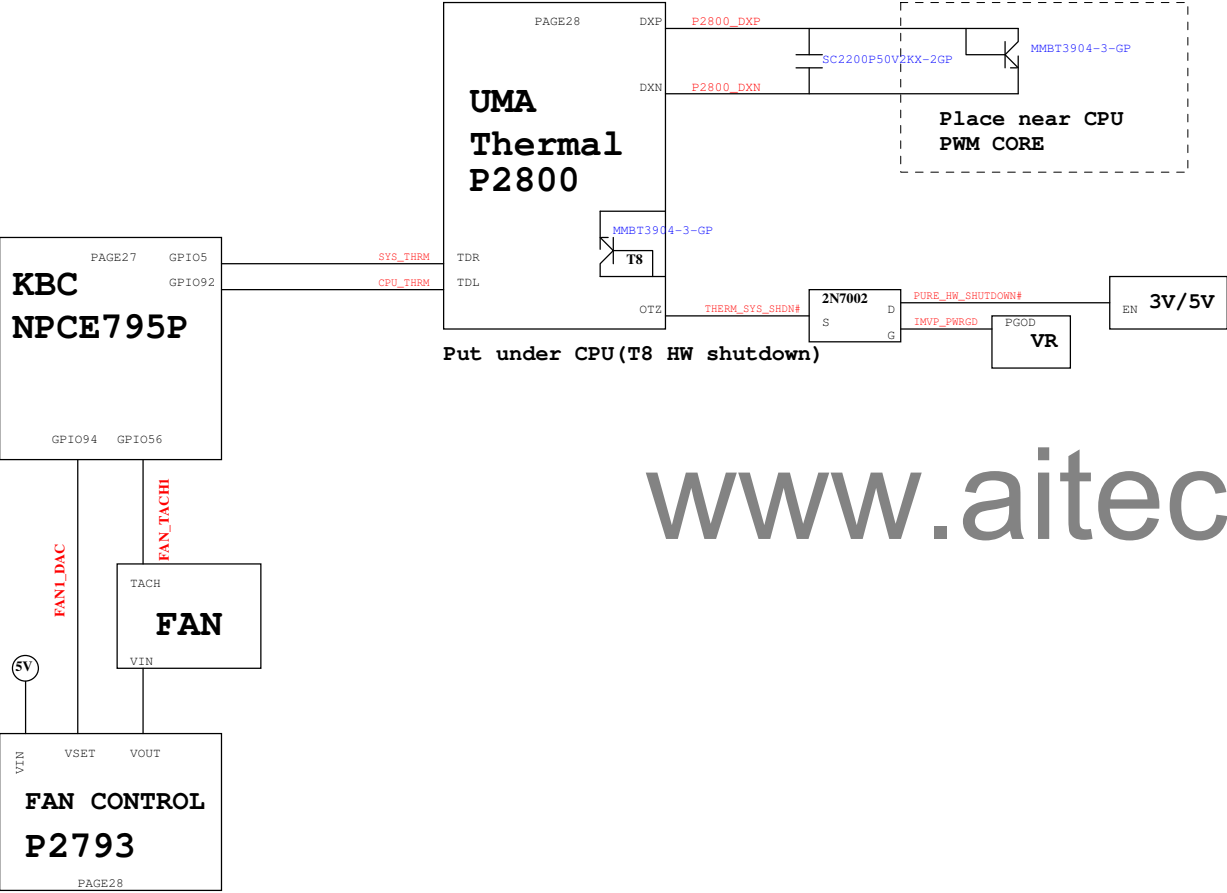


KBC SMBus Block Diagram



www.aitech1.ru

Thermal Block Diagram



Audio Block Diagram

